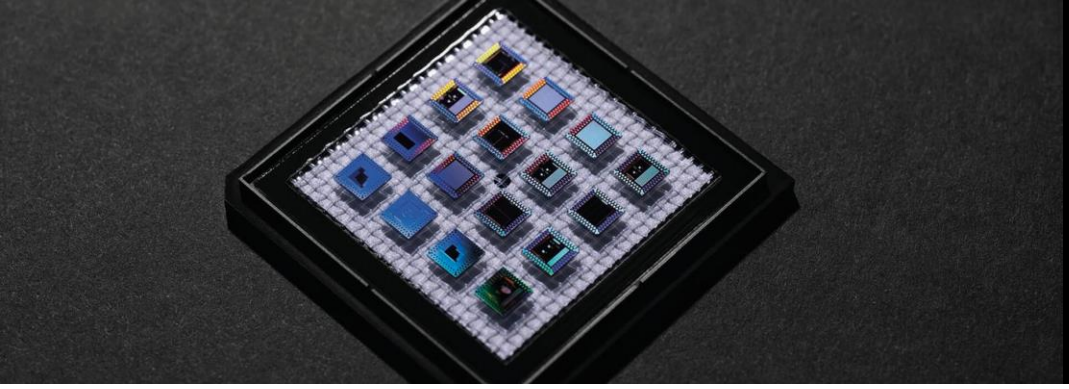
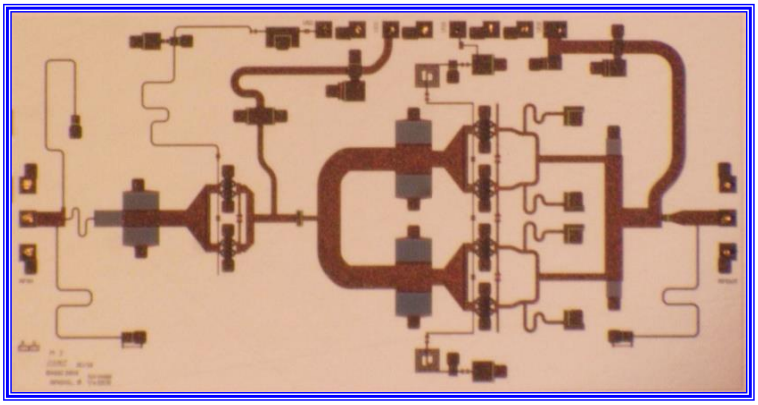


APN149
17 – 22 GHz
GaN Power Amplifier

*** PLEASE REFER TO GENERAL CHIP DIAGRAMS FOR TAB DIMENSIONING AND BONDING ***

PRODUCT DESCRIPTION

The APN149 monolithic GaN HEMT amplifier is a broadband, two-stage power device, designed for use in Point-to-Point and Multipoint Digital Radios, Military SatCom and Radar Applications. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.



X= 4.4 mm; Y= 2.28 mm

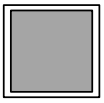
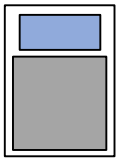
APPLICATIONS

- Military SatCom
- Phased-Array Radar Applications
- Point-to-Point Radio
- Point-to-Multipoint Communications
- Terminal Amplifiers

PRODUCT FEATURES

- RF frequency: 17 to 22 GHz
- Linear Gain: 20 dB typ.
- Psat: 38 dBm typ.
- Efficiency @ P3dB > 30 %
- Die Size: < 10.032 sq. mm.
- 0.2um GaN HEMT
- 4 mil SiC substrate
- DC Power: 28 VDC @ 544 mA

PRODUCT OPTIONS

OPTION	FIGURE	PART #
BARE DIE		APN149
BARE DIE + TAB		APN149TAB
BARE DIE + TAB + CAPACITOR		APN149TABC

EXPORT INFORMATION

ECCN: 3A001.b.2

HTS (Schedule B) code: 8542.33.0001

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APN149
17 – 22 GHz
GaN Power Amplifier

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Drain Voltage	28	V
Gate Voltage Range	-8 to 0	V
Drain Current	700	mA
Gate Current	0.3	mA
Soldering Temperature	320	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Unit
Drain Voltage Range	20 - 28	V
Gate Voltage Range	-5 to -3	V
Stg 1 Drain Current (Idq)	144	mA
Stg 2 Drain Current (Idq)	400	mA

ELECTRICAL SPECIFICATIONS

Parameter	Min	Typical	Max	Unit
Operational Frequency	17		22	GHz
Small Signal at 28V				
Small Signal Linear Gain	19	22	23.3	dB
Input Return Loss	-30		-4.2	dB
Output Return Loss	-26		-7.5	dB
On-Wafer Pulsed Power at 28V				
Psat (at 25 dBm)	39.3	39.7	40.3	dBm
Power Gain (at 25 dBm)	14.3	14.7	15.3	dB
P1db	38	38.2	38.4	dBm
PAE (at 25 dBm)	31.9	32.5	34.6	%
Max PAE	33.7	34.5	34.5	%
Fixtured CW at 28V, 25°C Case Temp				
Psat (at 22 dBm)	38.1	38.7	39.1	dBm
Power Gain (at 22 dBm)	16.2	16.8	17.2	dB
PAE (at 22 dBm)	28.3	29	33	%
Max PAE	28.3	29.1	33.2	%
Drain Voltage		28		V
Stage 1 Gate Voltage		-4.190		V
Stage 2 Gate Voltage		-4.190		V
Stage 1 Idq		144		mA
Stage 2 Idq		400		mA

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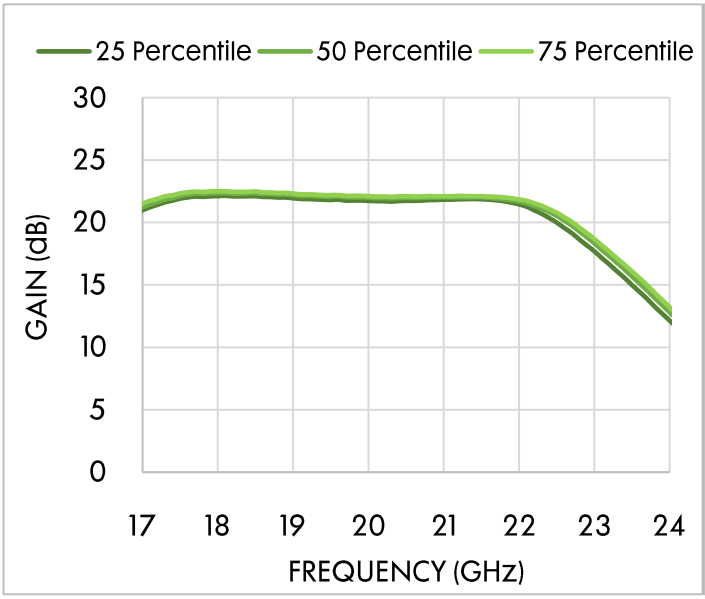
NORTHROP GRUMMAN

APN149
17 – 22 GHz
GaN Power Amplifier

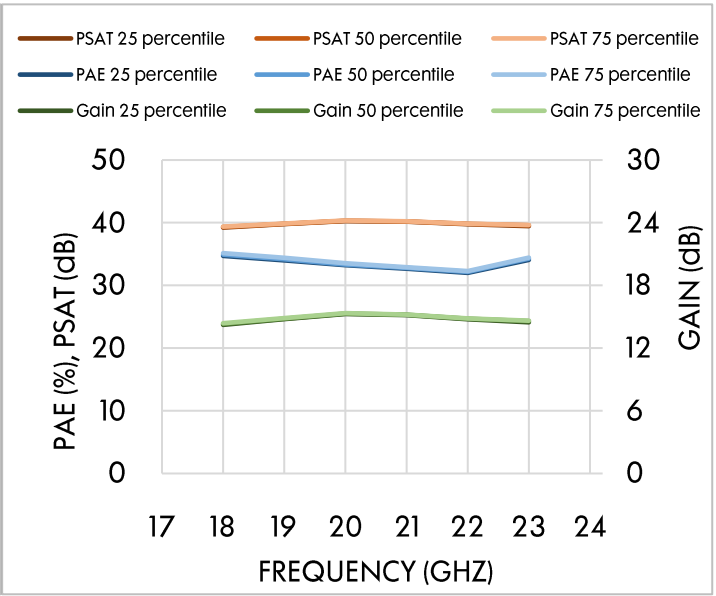
Pulsed On wafer measured Performance Characteristics (Typical Performance at 25°C)

Vd = 28.0 V, Id1 = 140 mA, Id2 = 400 mA. *

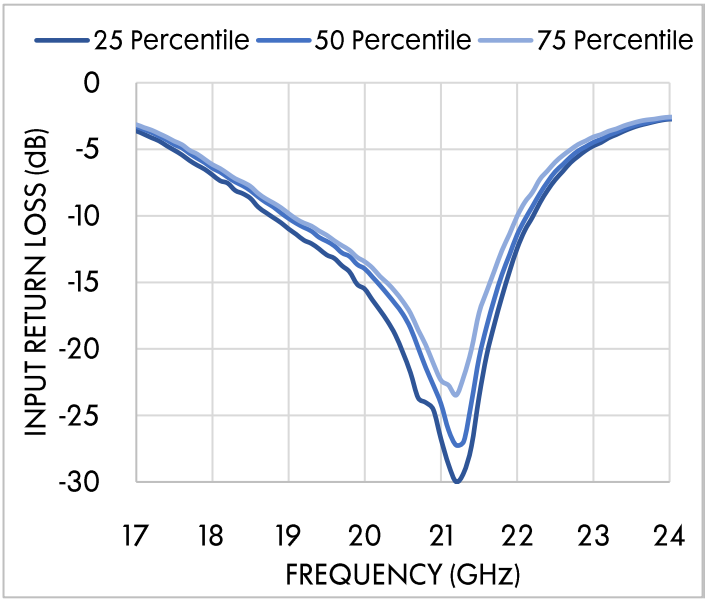
Small Signal Gain vs. Frequency



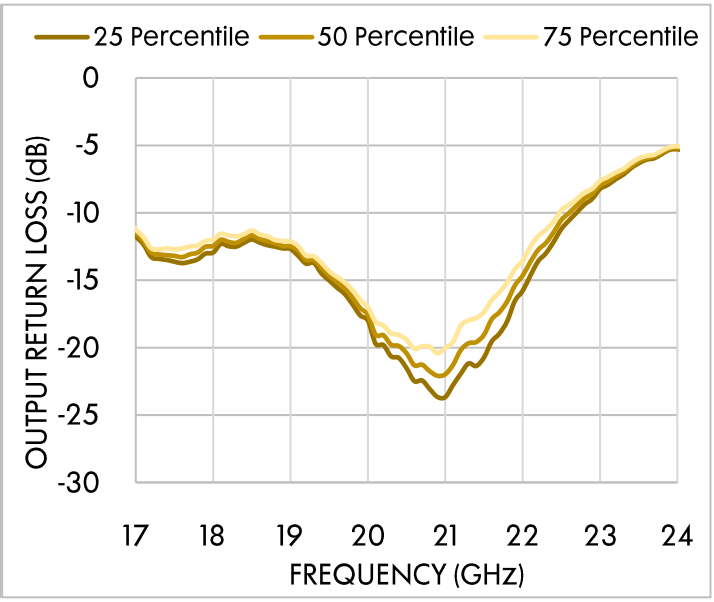
Large Signal PAE, Gain, PSAT vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



* Pulsed-power on-wafer

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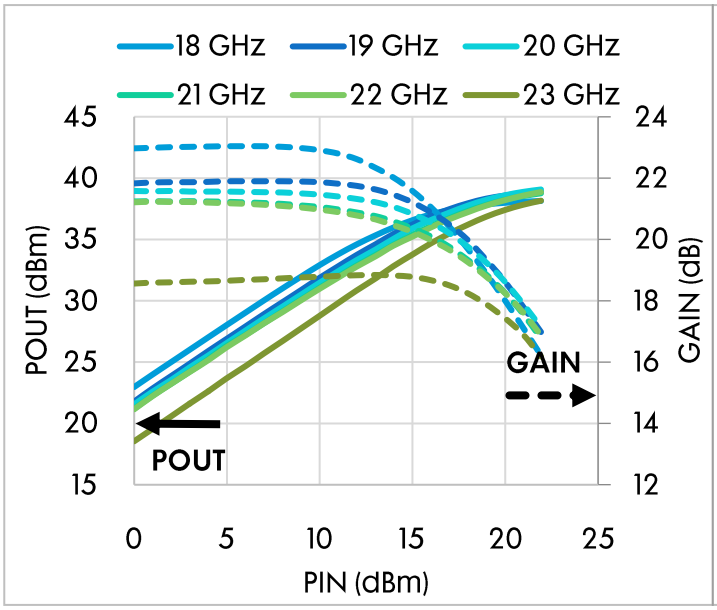
GaN Power Amplifier

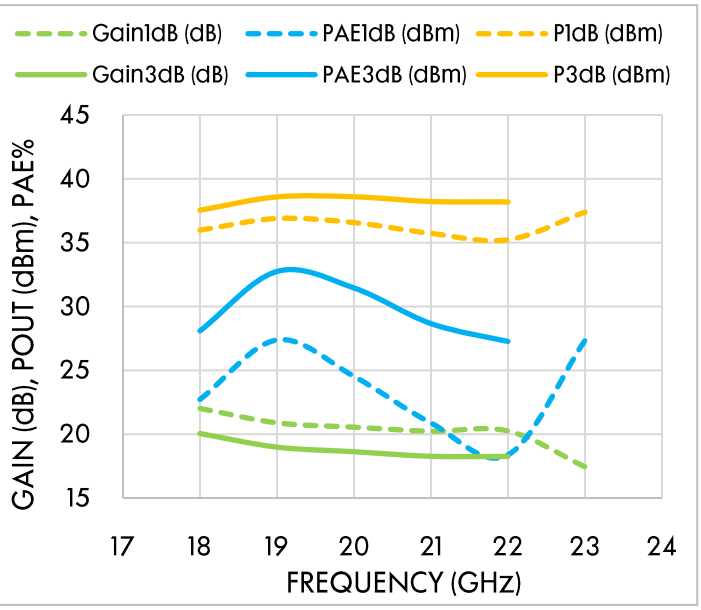
Fixture measured Performance Characteristics (Typical Performance at 25°C)

Vd = 28.0 V, Id1 = 144 mA, Id2 =400 mA

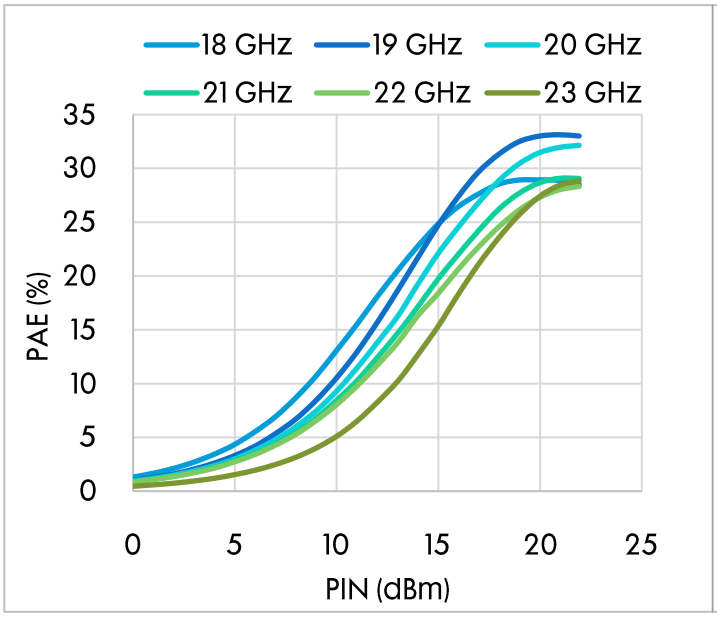
POUT and Gain vs. PIN



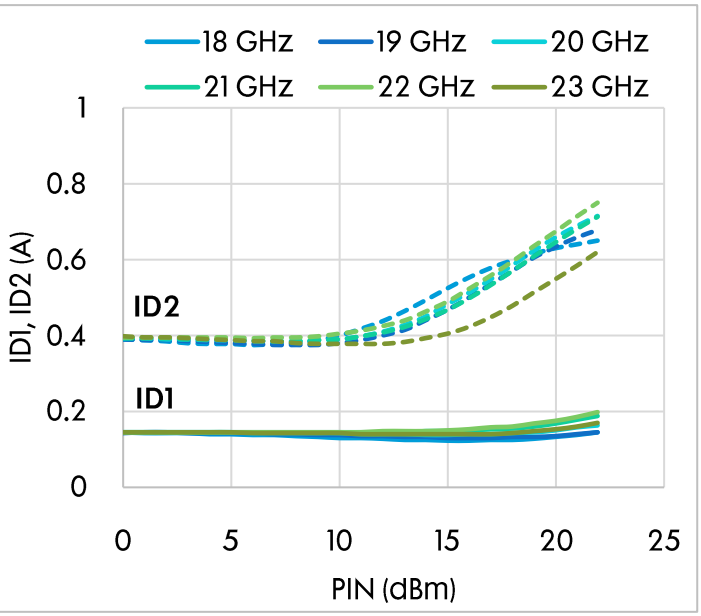
PAE, Gain, POUT vs. Frequency



PAE vs. PIN



ID1, ID2 vs. PIN



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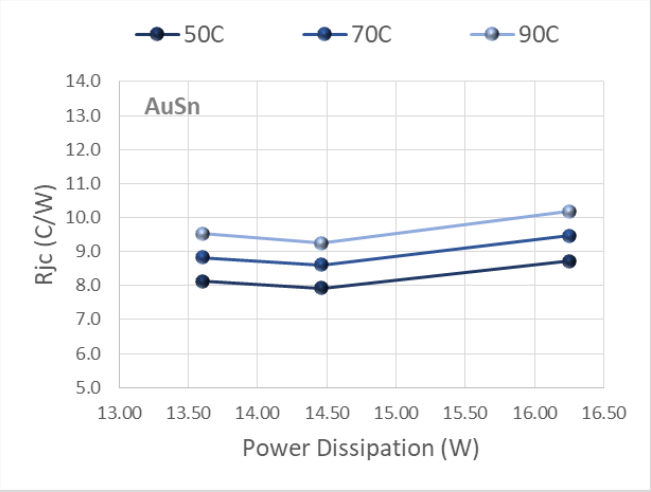
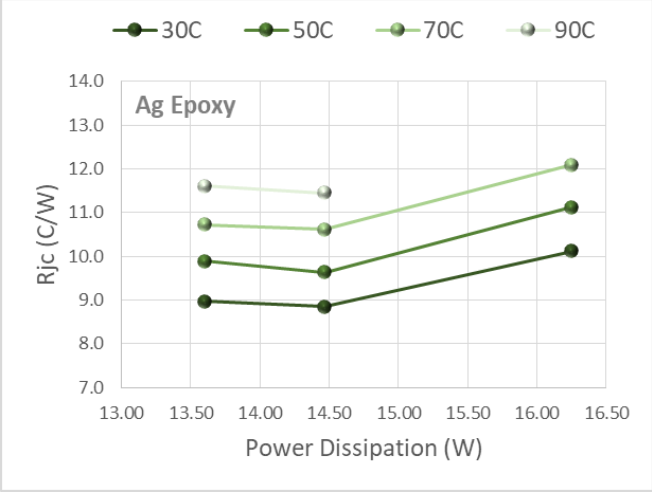
GaN Power Amplifier

Preliminary Thermal Properties with die mounted with 25um 80/20 AuSn Eutectic to: 10mil CuW10W Shim

Shim	Mounting Material	Average Backside Die Temperature	Hottest Junction Temperature Tjc	RF Output	Power Dissipation (W)	Thermal Resistance Rjc (°C/W)
10 mil CuW	AuSn Eutectic	50 °C	161	33.2	13.6	8.1
			164	36.4	14.5	7.9
			192	39.1	16.3	8.7
		70 °C	190	33.2	13.6	8.8
			194	36.4	14.5	8.6
			224	39.1	16.3	9.5
		90 °C	220	33.2	13.6	9.5
			224	36.4	14.5	9.2
			255	39.1	16.3	10.2
10 mil CuW	Ag Epoxy	30 °C	152	33.2	13.6	9
			158	36.4	14.5	8.8
			194	39.1	16.3	10.1
		50 °C	184	33.2	13.6	9.9
			189	36.4	14.5	9.6
			231	39.1	16.3	11.1
		70 °C	216	33.2	13.6	10.7
			223	36.4	14.5	10.6
			266	39.1	16.3	12.1
		90 °C	248	33.2	13.6	11.6
			257	36.4	14.5	11.5





** Vd = 28.0 V, Idq1 = 143 mA, Id2q = 375 mA

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APN149
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GaN Power Amplifier

DIE SIZE AND BOND PAD LOCATIONS

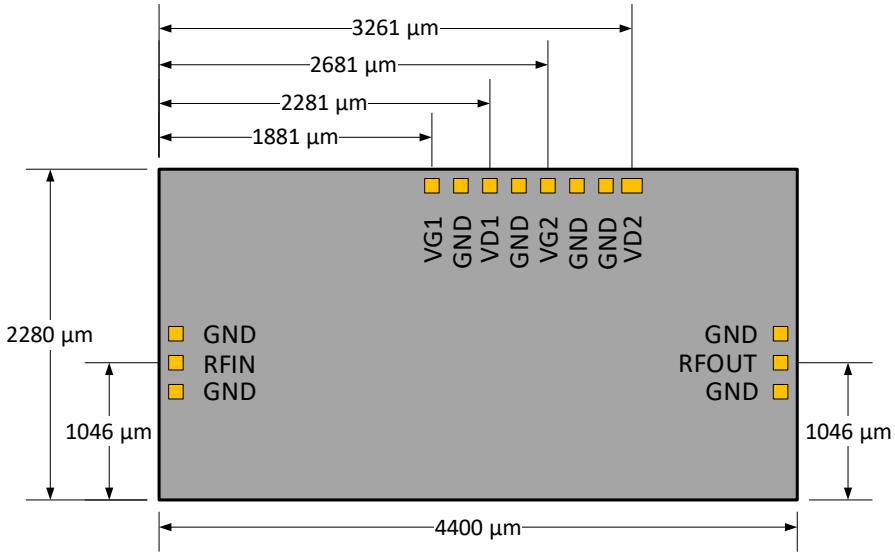
X =4400 µm ± 25 µm

Y = 2280 ± 25 µm

DC Bond Pad = 100 x 100 ± 0.5 µm

RF Bond Pad = 100 x 100 ± 0.5 µm

Chip Thickness = 101 ± 5 µm



BIASING/DE-BIASING DETAILS:

Bias for 1st stage is from top.

The 2nd stages must bias up from both sides.

Listed below are some guidelines for GaN device

testing and wire bonding:

a. Limited positive gate bias (G-S or G-D) to < 1V

b. Know your devices' breakdown voltages

c. Use a power supply with both voltage and current limit

d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture
    a. Apply negative gate voltage (-8 V) to ensure that all devices are off
    b. Ramp up drain bias to ~10 V
    c. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    d. Ramp up drain to operating bias
    e. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved

e. To safely de-bias GaN devices, start by de-biasing output amplifier stages first (if applicable):
    a. Set gate voltage back to pinch-off (-8 V)
    b. Gradually decrease drain bias to 0 V
    c. Gradually decrease gate bias to 0 V
    d. Turn off supply voltages

f. Repeat de-bias procedure for each amplifier stage

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TAB-DIE SIZE AND BOND PAD LOCATIONS

CuMoCu-based Tab

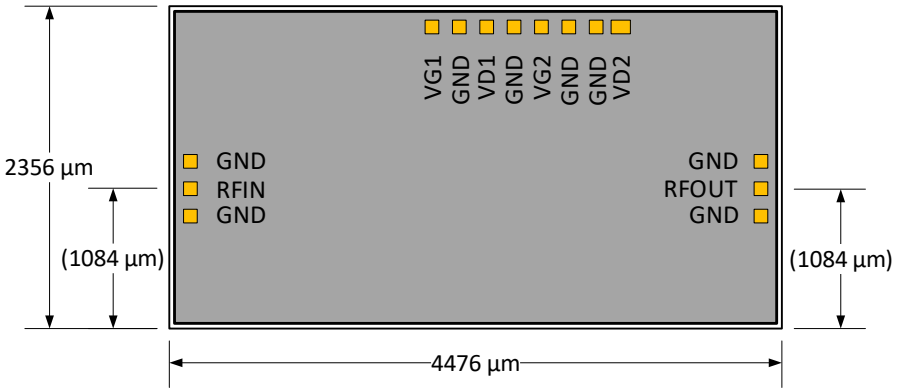
X = 4476 µm ± 25 µm

Y = 2356 µm ± 25 µm

Tab Thickness = 254 µm ± 25 µm

Eutectic Solder layer

Eutectic Thickness = 25 µm (1 mil) nominal



APN149TAB

TAB-CAPACITOR-DIE SIZE AND BOND PAD LOCATIONS

CuMoCu-based Tab + Capacitor

X = 4476 µm ± 25 µm

Y = 3488 µm ± 25 µm

Tab Thickness = 254 µm ± 25 µm

Eutectic Solder layer

Eutectic Thickness = 25 µm (1 mil) nominal

100pF, 100V Bar Capacitors

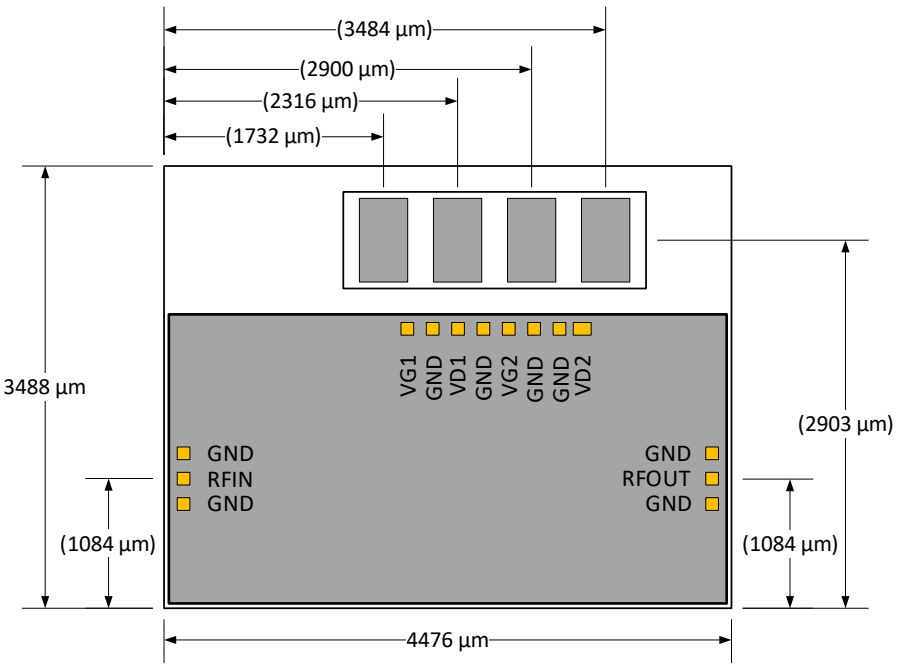
X = 2388 µm ± 76 µm

Y = 762 µm ± 76 µm

DC Gold Bond Pad = 381 x 660 µm nominal

Cap Thickness = 127 µm ± 38 µm

Cap Part Number = CRM-BN-94X30X5-G-101-Z-CE396 (or equivalent)



APN149TABC

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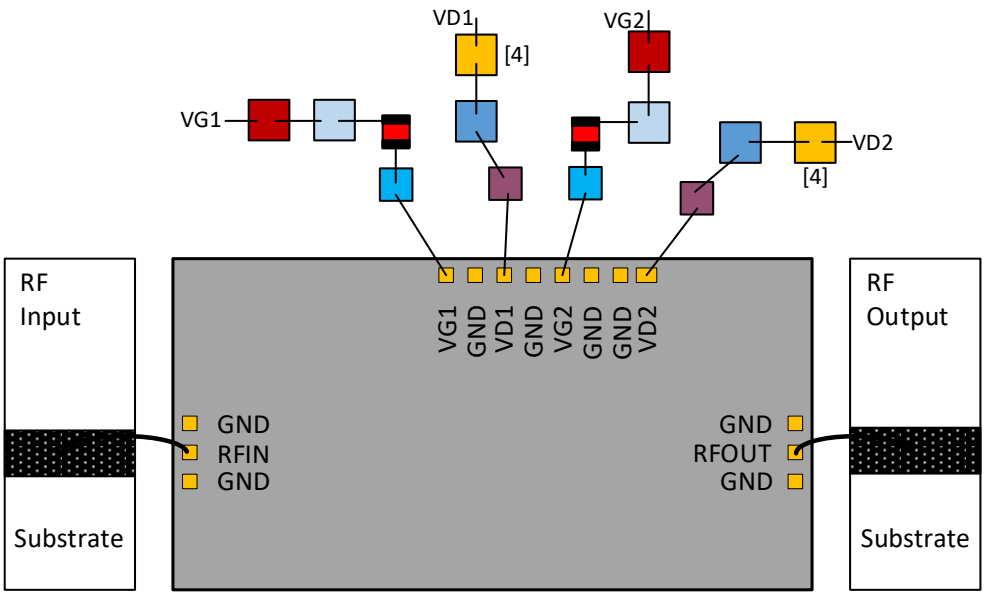
APN149
17 – 22 GHz
GaN Power Amplifier

RECOMMENDED ASSEMBLY NOTES

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

SUGGESTED BONDING ARRANGEMENT



GENERAL DIAGRAM SYMBOLS

= 0.1 uF, 50V (Shunt) [4]

= 0.1 uF, 15V (Shunt)

= 100 pF, 50V (Shunt)

= 0.01 uF, 50V (Shunt)

= 0.01 uF, 15V (Shunt)

= 100 pF, 15V (Shunt)

= 10 Ohms, 30V (Series)

MOUNTING PROCESSES

Most NGSS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGSS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320 °C for 30 seconds.

Note: Many of the NGSS parts do incorporate airbridges, so caution should be used when determining the pickup tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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GENERAL CHIP DIAGRAM FOR DIMENSIONING

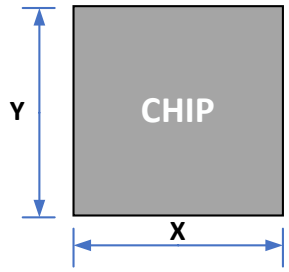

Figure A

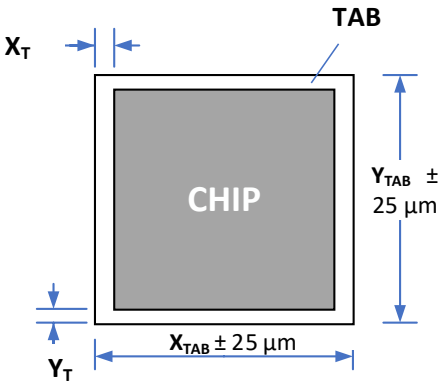

Figure B

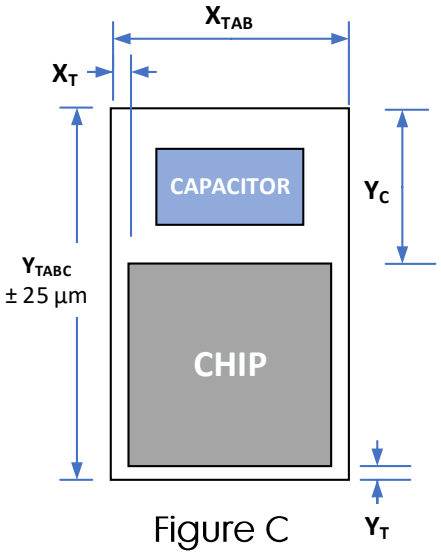

Figure C

SCHEMATIC LEGEND

Parameter	Value	Tolerance
Chip Width (X)	See Die Size Page	See Die Size Page
Chip Length (Y)	See Die Size Page	See Die Size Page
Tab-Chip Width Offset (X_T)	38 µm (0.0015″)	-
Tab-Chip Length Offset (Y_T)	38 µm (0.0015″)	-
TAB Width (X_{TAB})	$X_{TAB} = X + 76$ µm	± 25 µm
TAB Length (Y_{TAB})	$Y_{TAB} = Y + 76$ µm	± 25 µm
TAB Length (Y_{TABC})	$Y_{TABC} = Y + Y_C + Y_T$	± 25 µm
Chip Edge to TAB Edge Length (Y_C)	1170 µm (0.046″)	-

NOTES

Figure A: Chip

Figure B: Chip + Heat Spreader (TAB)

Figure C: Chip + Heat Spreader (TAB) + Capacitor

- Chip Width and Length vary depending on product dimensions

- Each Parameter has its own respective tolerance that is shown throughout the data sheet

- Figures B and C have the same Width (X_{TAB})

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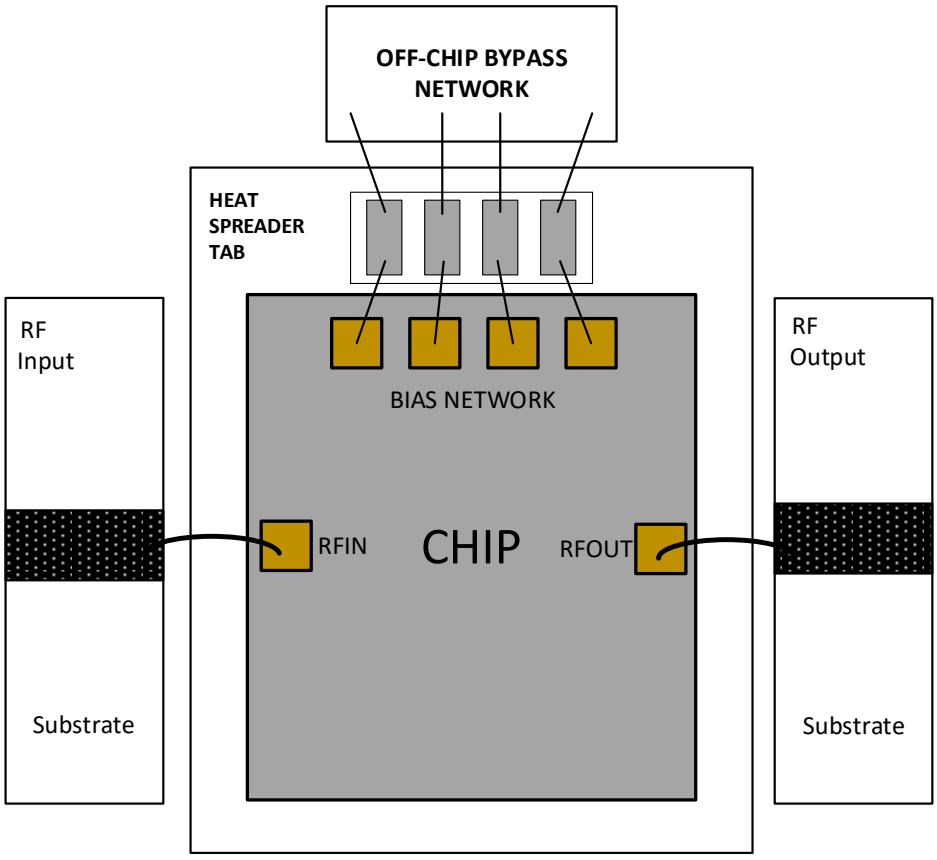
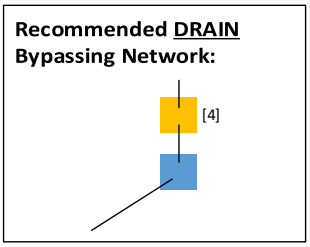
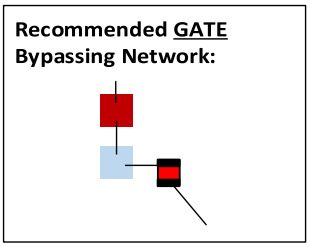
GENERAL BONDING ARRANGEMENT FOR FIGURE C

** BELOW LAYOUT SHOWS BONDING ARRANGEMENT OF A GENERIC AMPLIFIER FOR REFERENCE

** SPECIFIC BYPASS INTERCONNECTIONS DRIVEN BY RESPECTIVE CHIP







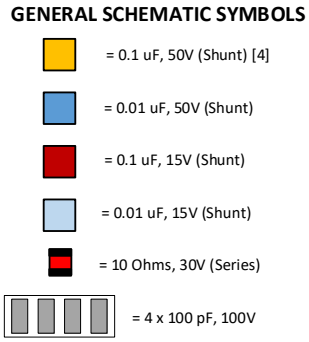


DIAGRAM NOTES

- The 100 pF (15V & 50V) capacitors shown in the "SUGGESTED BONDING ARANGEMENT" Bare Die diagram are replaced with 100 pF (100V) Bar Capacitors for the Capacitor TAB configuration

- The remaining capacitors/resistors previously shown in "SUGGESTED BONDING ARANGEMENT" are the same and now connect to the Bar Capacitors

- Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.

- [4] The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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