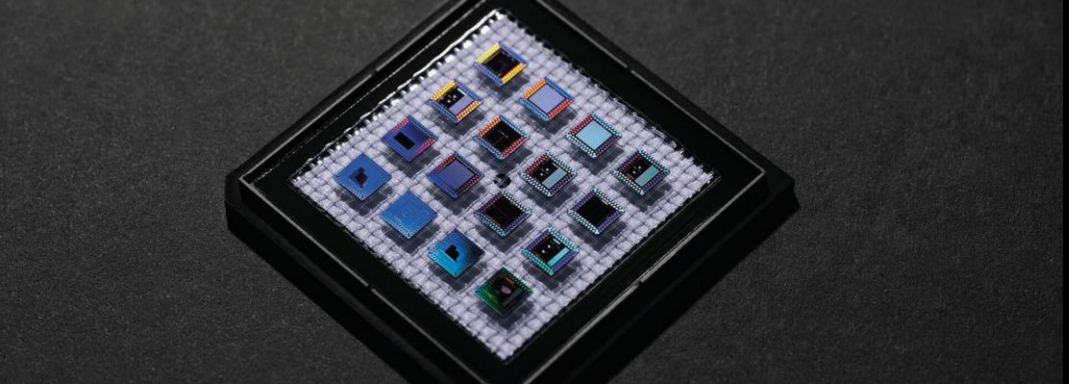
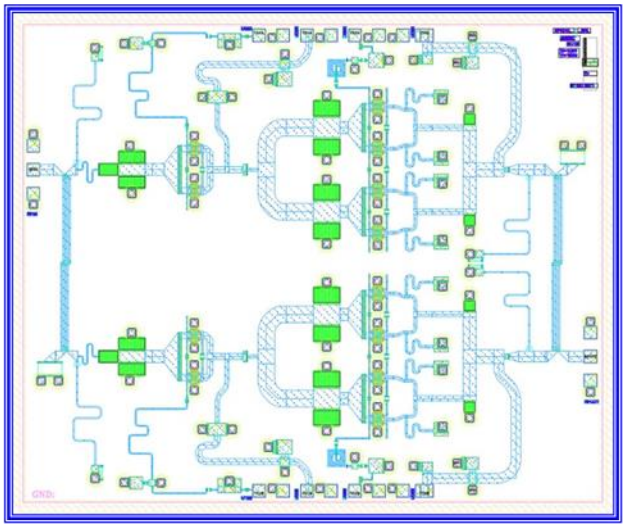


APN187
17 – 22 GHz
GaN Power Amplifier

*** PLEASE REFER TO GENERAL CHIP DIAGRAMS FOR TAB DIMENSIONING AND BONDING ***

PRODUCT DESCRIPTION

The APN187 monolithic GaN HEMT amplifier is a broadband, two-stage power device, designed for use in Point-to-Point and Multipoint Digital Radios, Military SatCom and Radar Applications. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.



X= 4.8 mm; Y= 4.02 mm

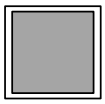
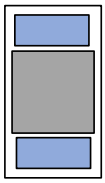
APPLICATIONS

- Military SatCom
- Phased-Array Radar Applications
- Point-to-Point Radio
- Point-to-Multipoint Communications
- Terminal Amplifiers

PRODUCT FEATURES

- RF frequency: 17 to 22 GHz
- Linear Gain: 20 dB typ.
- Psat: 41 dBm typ.
- Efficiency @ P3dB >28 %
- Die Size: < 19.845 sq. mm.
- 0.2um GaN HEMT
- 4 mil SiC substrate
- DC Power: 28 VDC @ 1088 mA

PRODUCT OPTIONS

OPTION	FIGURE	PART #
BARE DIE		APN187
BARE DIE + TAB		APN187TAB
BARE DIE + TAB + CAPACITORS		APN187TABC

EXPORT INFORMATION

ECCN: 3A001.b.2

HTS (Schedule B) code: 8542.33.0001

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APN187
17 – 22 GHz
GaN Power Amplifier

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Drain Voltage	28	V
Gate Voltage Range	-8 to 0	V
Drain Current	1400	mA
Gate Current	0.6	mA
Soldering Temperature	320	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Unit
Drain Voltage Range	20 - 28	V
Gate Voltage Range	-5 to -3	V
Stg 1 Drain Current (Idq)	288	mA
Stg 2 Drain Current (Idq)	800	mA

ELECTRICAL SPECIFICATIONS

Parameter	Min	Typical	Max	Unit
Operational Frequency	17		31	GHz
Small Signal at 28V				
Small Signal Linear Gain	19	21.8	22.3	dB
Input Return Loss	-26		-16	dB
Output Return Loss	-30		-16	dB
On-Wafer Pulsed Power at 28V				
Psat (at 25 dBm)	40	41.8	42.5	dBm
Power Gain (at 25 dBm)	15.5	16.9	17.5	dB
P1db	38.5	39.8	40.6	dBm
PAE (at 25 dBm)	26.5	28	33.2	%
Max PAE	27.6	28.5	34	%
Fixtured CW at 28V, 25°C Case Temp				
Psat (at 25 dBm)	40.1	42.1	42.5	dBm
Power Gain (at 25 dBm)	15.1	17.2	17.5	dB
PAE (at 25 dBm)	26.5	31.5	34.2	%
Max PAE	29.5	32	34.6	%
Drain Voltage		28		V
Stage 1 Gate Voltage		-4.190		V
Stage 2 Gate Voltage		-4.130		V
Stage 1 Idq		288		mA
Stage 2 Idq		800		mA

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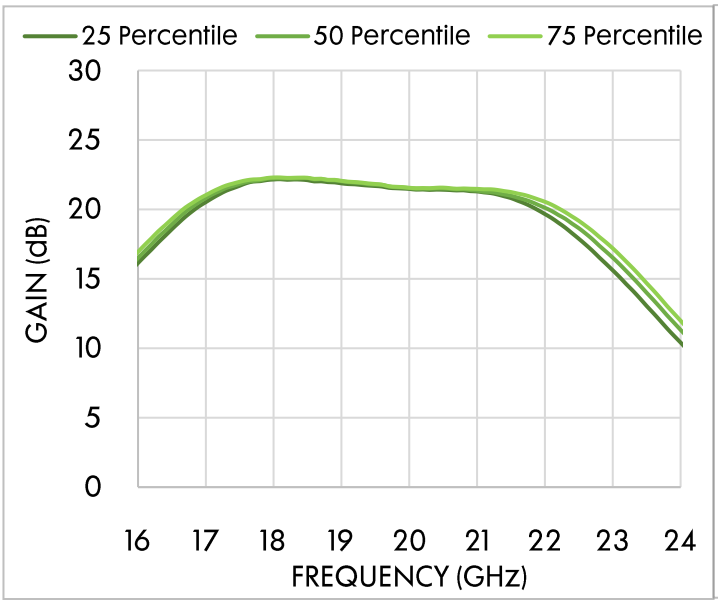
APN187
17 – 22 GHz
GaN Power Amplifier

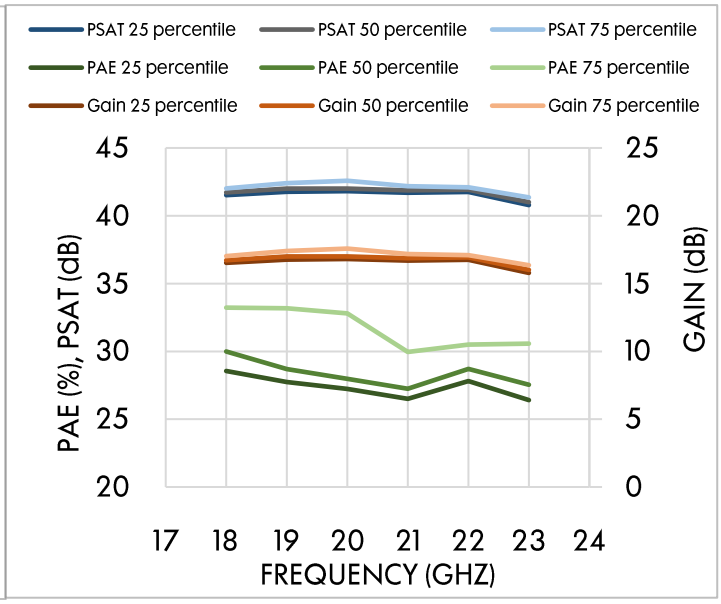
Pulsed On wafer measured Performance Characteristics (Typical Performance at 25°C)

Vd= 28.0 V, Id1+Id1a = 288 mA, Id2+Id2a = 800 mA. *

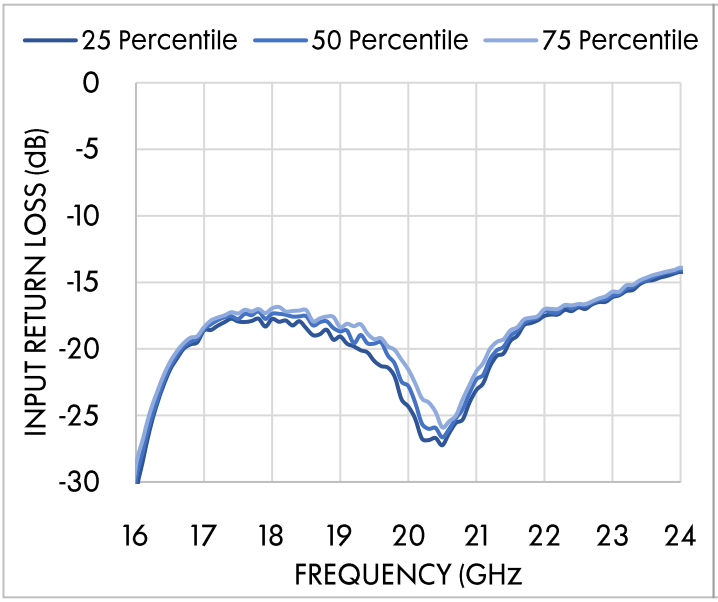
Small Signal Gain vs. Frequency



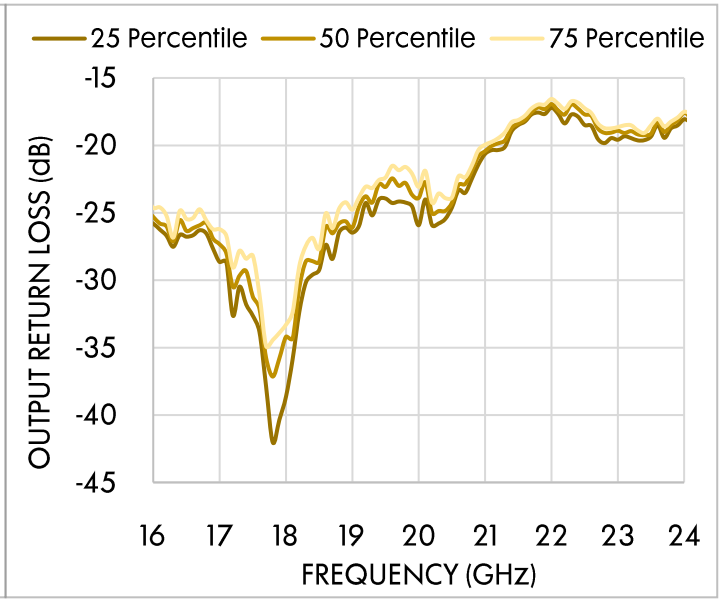
Large Signal PAE, Gain, PSAT vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



* Pulsed-power on-wafer

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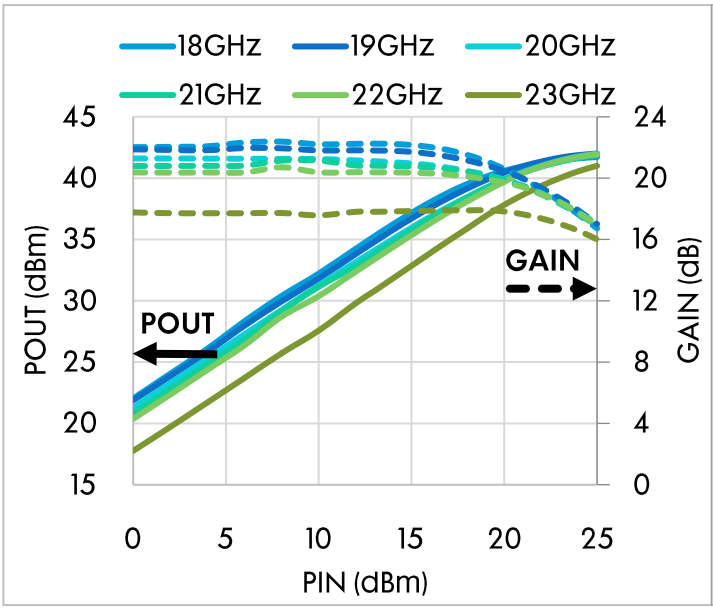
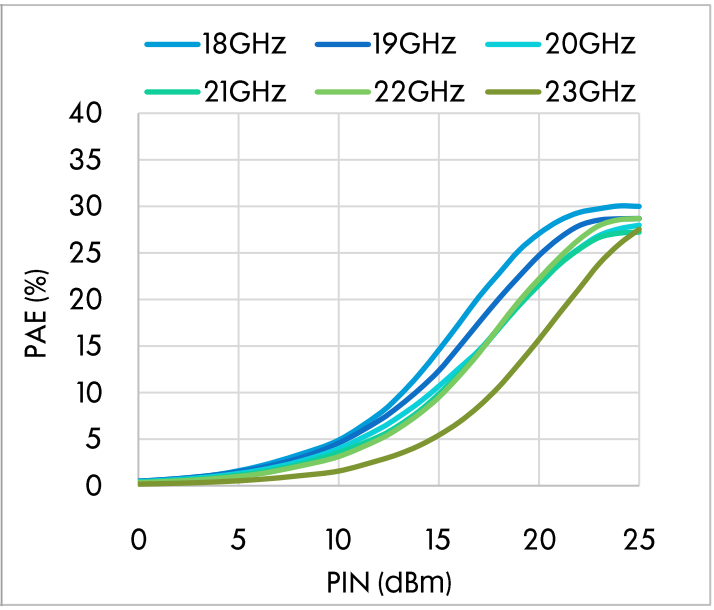
Pulsed On wafer measured Performance Characteristics (Typical Performance at 25°C)

Vd= 28.0 V, Id1+Id1a = 288 mA, Id2+Id2a = 800 mA. *

Large Signal Gain, POUT vs. Power, PIN	Large Signal PAE vs. Power, PIN





* Pulsed-power on-wafer

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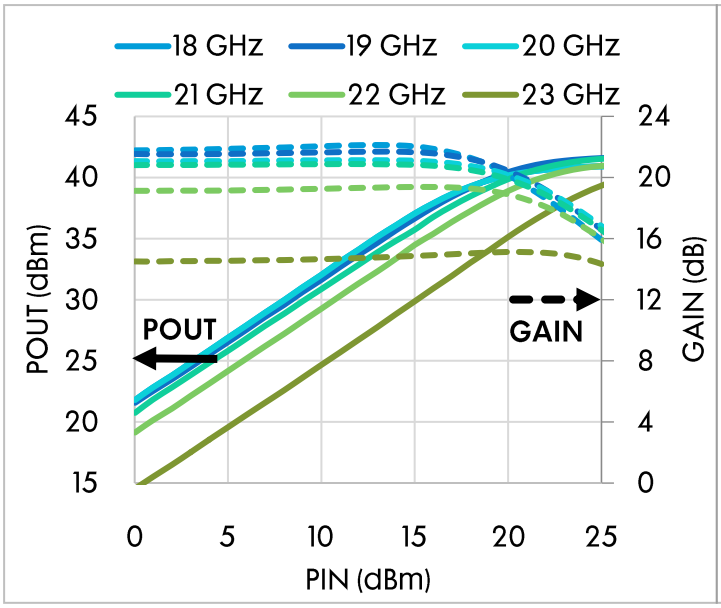
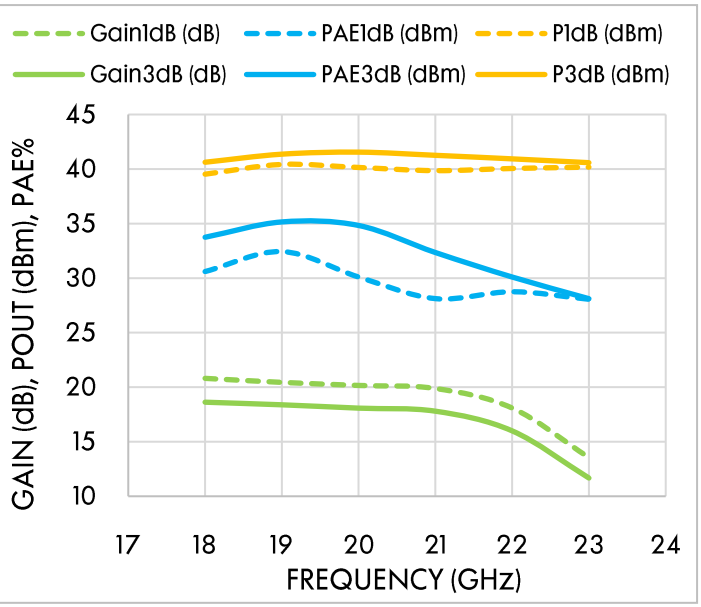
Fixture measured Performance Characteristics (Typical Performance at 25°C)

Vd = 24.0 V, Id1 = 288 mA, Id2 =800 mA

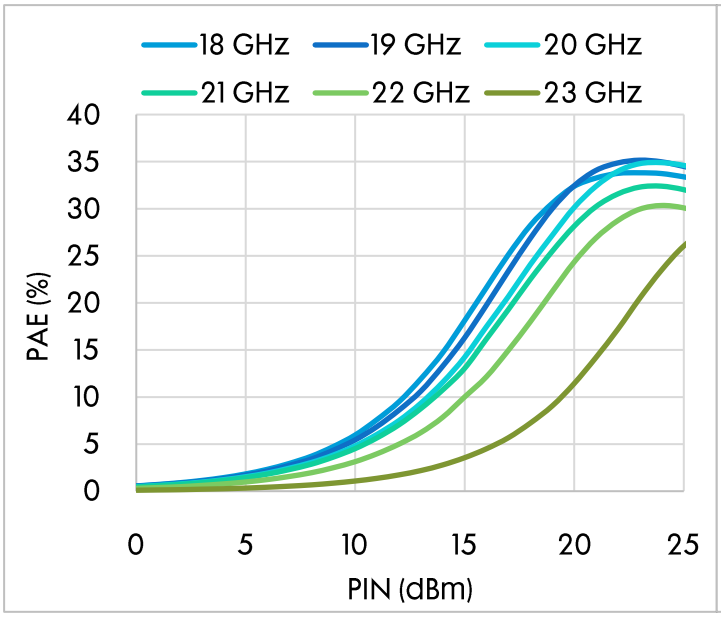
POUT and Gain vs. PIN



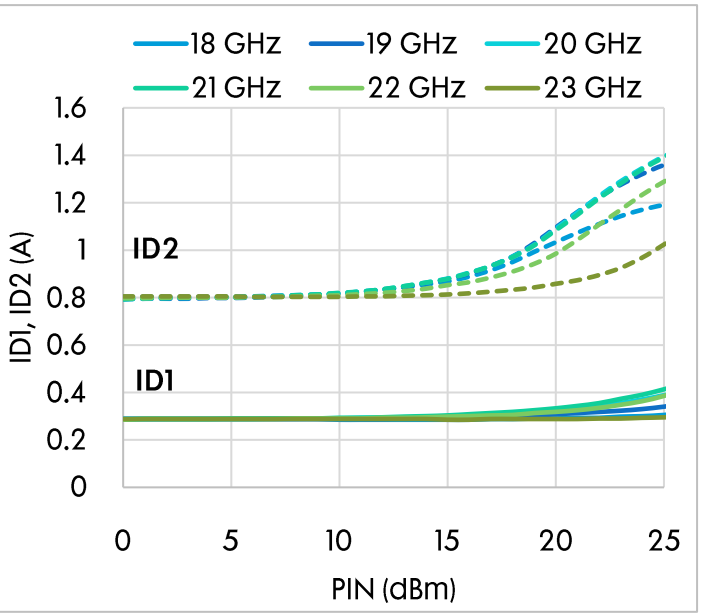
PAE, Gain, POUT vs. Frequency



PAE vs. PIN



ID1, ID2 vs. PIN



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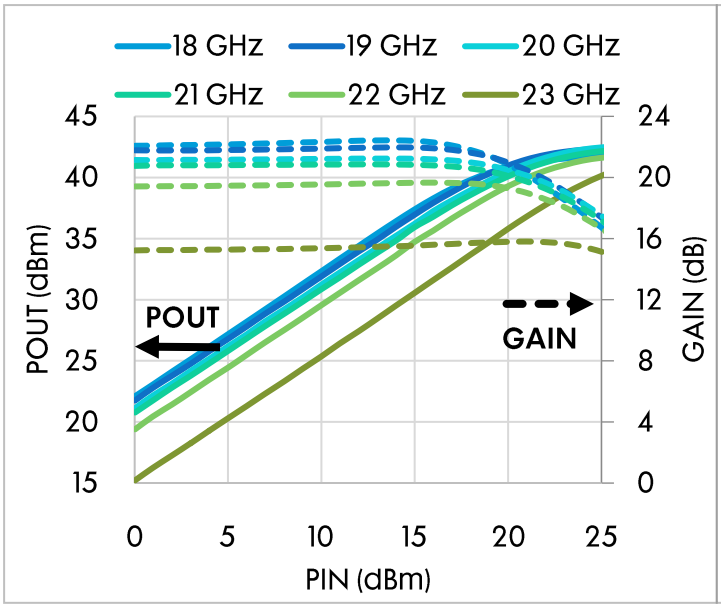
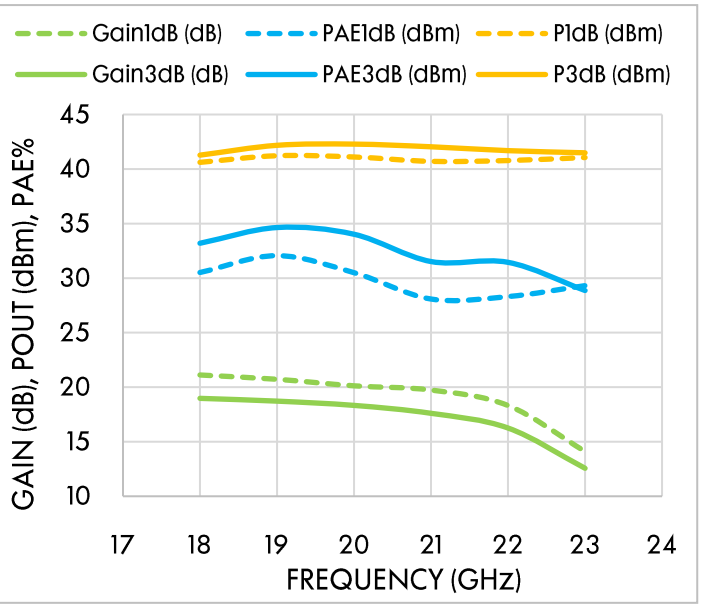
Fixture measured Performance Characteristics (Typical Performance at 25°C)

Vd = 28.0 V, Id1 = 288 mA, Id2 =800 mA

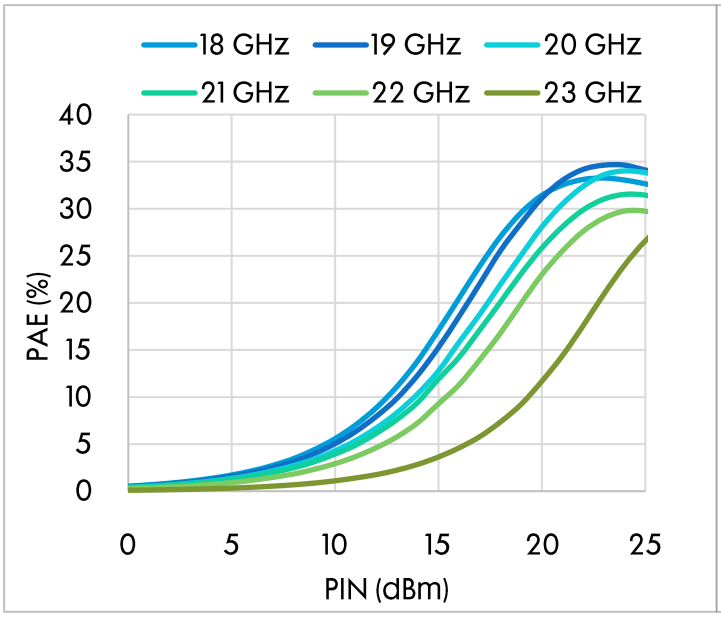
POUT and Gain vs. PIN



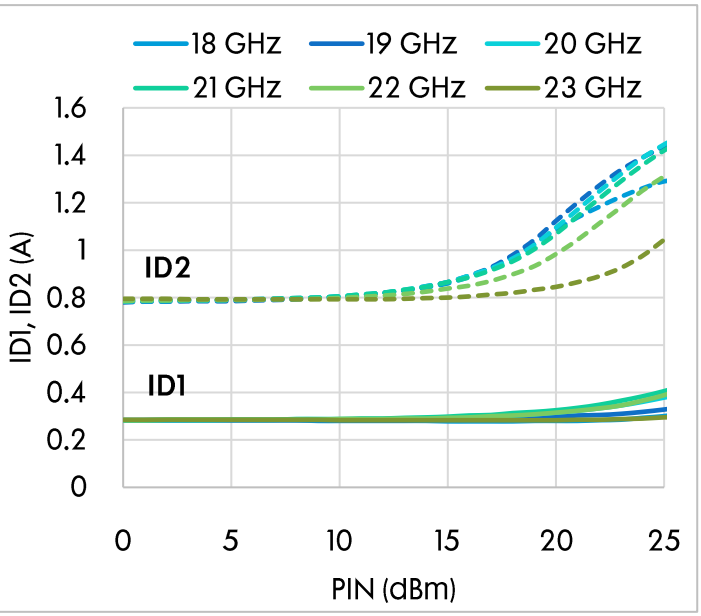
PAE, Gain, POUT vs. Frequency



PAE vs. PIN



ID1, ID2 vs. PIN



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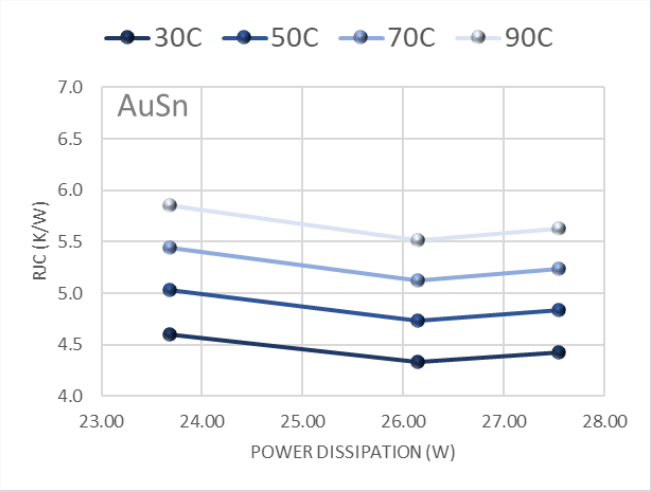
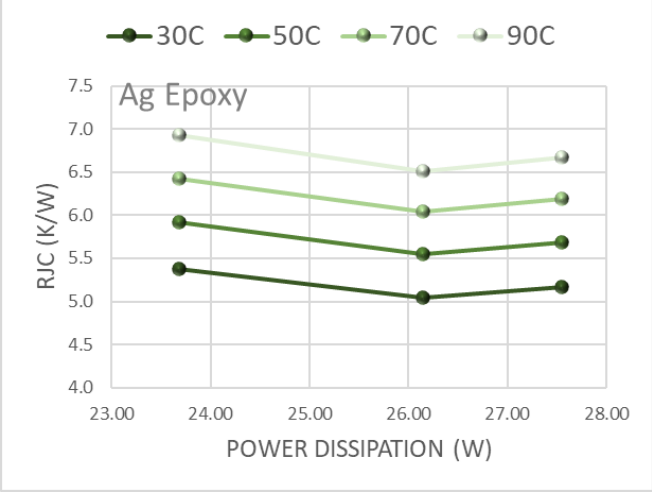
GaN Power Amplifier

Preliminary Thermal Properties with die mounted with 30 um 80/20 AuSn Eutectic ** to: 25 mil CuW85 Shim

Shim	Mounting Material	Average Backside Die Temperature	Hottest Junction Temperature Tjc	RF Output (dBm)	Power Dissipation (W)	Thermal Resistance Rjc (°C/W)
25 mil CuW	AuSn Eutectic	30 °C	139	42.0	23.68	4.6
			143	39.2	26.15	4.3
			152	36.2	27.55	4.4
		50 °C	169	42.0	23.68	5.0
			174	39.2	26.15	4.7
			183	36.2	27.55	4.8
		70 °C	199	42.0	23.68	5.4
			204	39.2	26.15	5.1
			214	36.2	27.55	5.2
		90 °C	229	42.0	23.68	5.9
			234	39.2	26.15	5.5
			245	36.2	27.55	5.6
25 mil CuW	Silver Epoxy	30 °C	157	42.0	23.68	5.4
			162	39.2	26.15	5.0
			172	36.2	27.55	5.2
		50 °C	190	42.0	23.68	5.9
			195	39.2	26.15	5.6
			207	36.2	27.55	5.7
		70 °C	222	42.0	23.68	6.4
			228	39.2	26.15	6.0
			240	36.2	27.55	6.2
		90 °C	254	42.0	23.68	6.9
			260	39.2	26.15	6.5
			274	36.2	27.55	6.7





** Vd = 28.0 V, Idq1 = 288 mA, Id2q = 800 mA

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DIE SIZE AND BOND PAD LOCATIONS

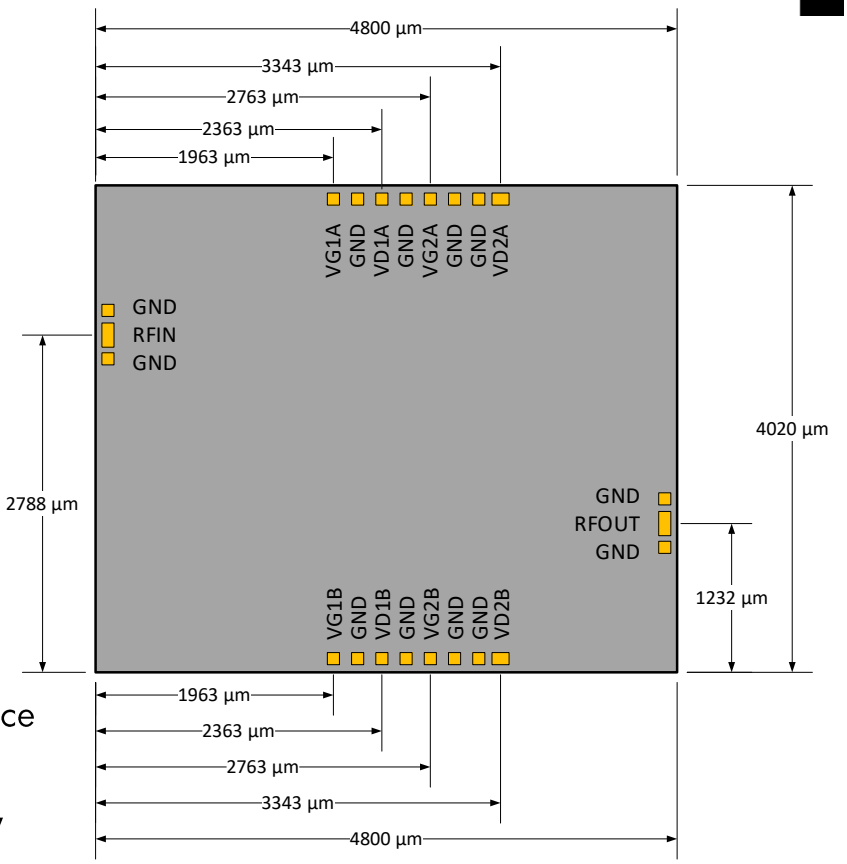
X =4800 µm ± 25 µm

Y = 4020 ± 25 µm

DC Bond Pad = 100 x 100 ± 0.5 µm

RF Bond Pad = 200 x 100 ± 0.5 µm

Chip Thickness = 101 ± 5 µm



BIASING/DE-BIASING DETAILS:

Bias for 1st stage is from top.

The 2nd stages must bias up from both sides.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limited positive gate bias (G-S or G-D) to < 1V

b. Know your devices' breakdown voltages

c. Use a power supply with both voltage and current limit

d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture
    a. Apply negative gate voltage (-8 V) to ensure that all devices are off
    b. Ramp up drain bias to ~10 V
    c. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    d. Ramp up drain to operating bias
    e. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved

e. To safely de-bias GaN devices, start by de-biasing output amplifier stages first (if applicable):
    a. Set gate voltage back to pinch-off (-8 V)
    b. Gradually decrease drain bias to 0 V
    c. Gradually decrease gate bias to 0 V
    d. Turn off supply voltages

f. Repeat de-bias procedure for each amplifier stage

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TAB-DIE SIZE AND BOND PAD LOCATIONS

CuMoCu-based Tab

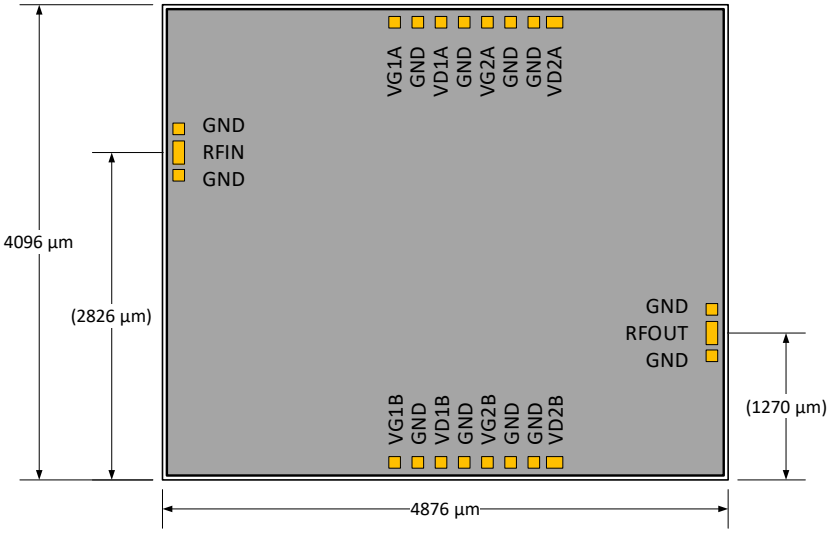
X = 4876 µm ± 25 µm

Y = 4096 µm ± 25 µm

Tab Thickness = 254 µm ± 25 µm

Eutectic Solder layer

Eutectic Thickness = 1 mil (25 µm) nominal



APN187TAB

TAB-CAPACITOR-DIE SIZE AND BOND PAD LOCATIONS

CuMoCu-based Tab + Capacitors

X = 4876 µm ± 25 µm

Y = 5775 µm ± 25 µm

Tab Thickness = 254 µm ± 25 µm

Eutectic Solder layer

Eutectic Thickness = 1 mil (25 µm) nominal

100pF, 100V Bar Capacitors

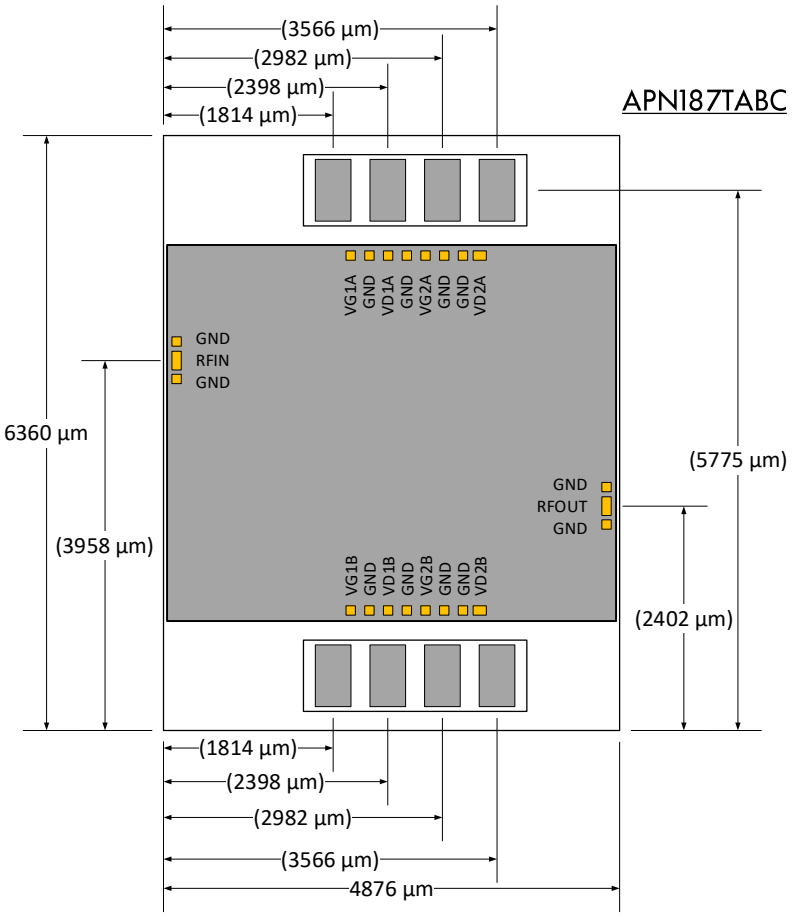
X = 2388 µm ± 76 µm

Y = 762 µm ± 76 µm

DC Gold Bond Pad = 381 x 660 µm nominal

Cap Thickness = 127 µm ± 38 µm

Cap Part Number = CRM-BN-94X30X5-G-101-Z-CE396 (or equivalent)



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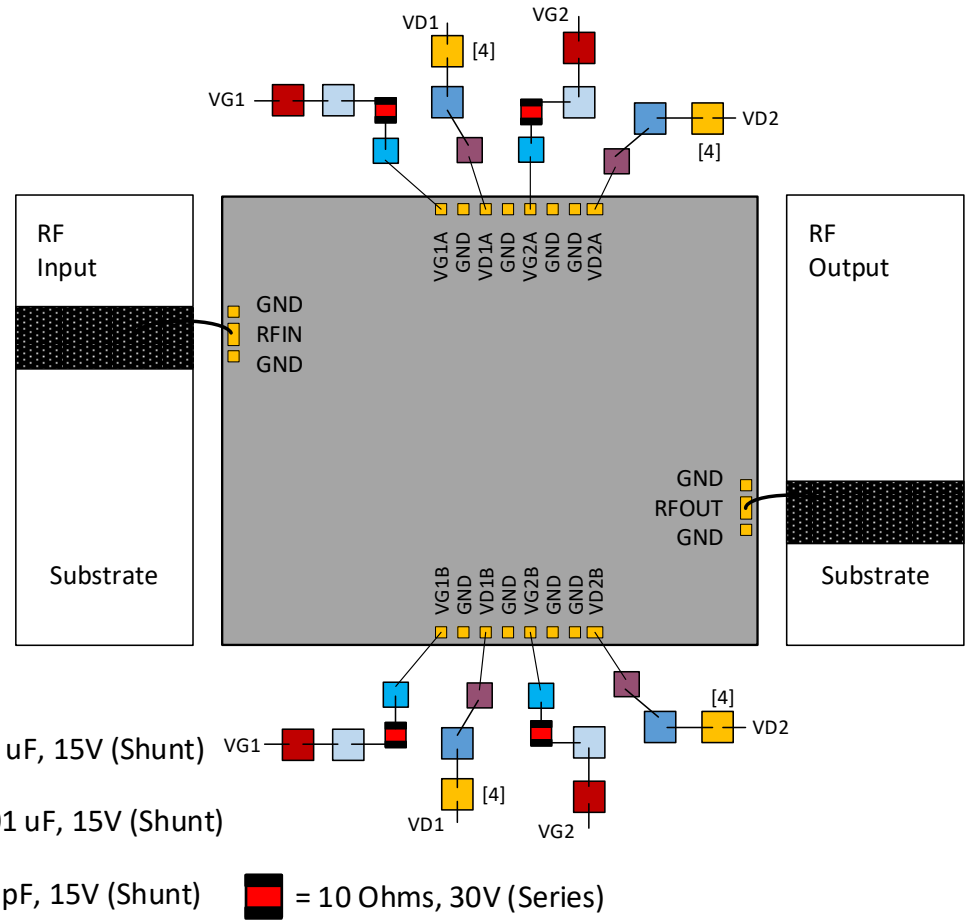
GaN Power Amplifier

RECOMMENDED ASSEMBLY NOTES

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

SUGGESTED BONDING ARRANGEMENT



GENERAL DIAGRAM SYMBOLS

= 0.1 uF, 50V (Shunt) [4]

= 0.1 uF, 15V (Shunt)

= 0.01 uF, 50V (Shunt)

= 0.01 uF, 15V (Shunt)

= 100 pF, 50V (Shunt)

= 100 pF, 15V (Shunt)

= 10 Ohms, 30V (Series)

MOUNTING PROCESSES

Most NGSS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGSS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320 °C for 30 seconds.

Note: Many of the NGSS parts do incorporate airbridges, so caution should be used when determining the pickup tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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GENERAL CHIP DIAGRAM FOR DIMENSIONING

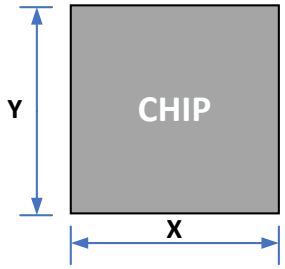

Figure A

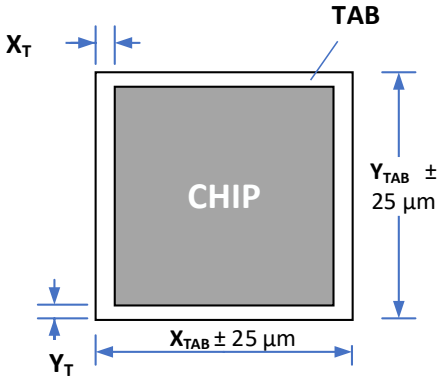

Figure B

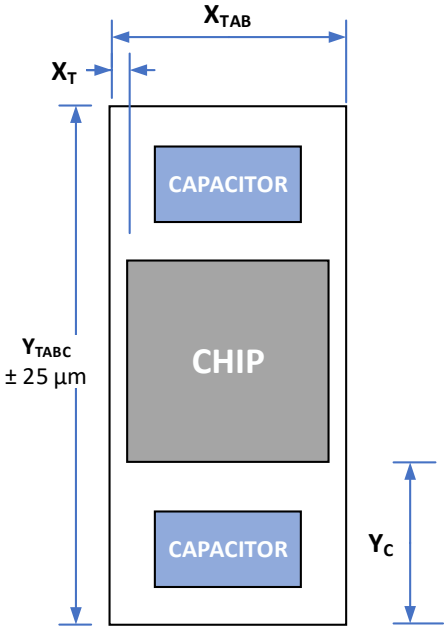

Figure C

SCHEMATIC LEGEND

Parameter	Value	Tolerance
Chip Width (X)	See Die Size Page	See Die Size Page
Chip Length (Y)	See Die Size Page	See Die Size Page
Tab-Chip Width Offset (X_T)	38 µm (0.0015″)	-
Tab-Chip Length Offset (Y_T)	38 µm (0.0015″)	-
TAB Width (X_{TAB})	$X_{TAB} = X + 76$ µm	± 25 µm
TAB Length (Y_{TAB})	$Y_{TAB} = Y + 76$ µm	± 25 µm
Chip Edge to TAB Edge Length (Y_C)	1170 µm (0.046″)	-
Tab-Chip-Capacitor Length (Y_{TABC})	$Y_{TABC} = Y + 2 \cdot Y_C$	± 25 µm

NOTES

Figure A: Chip

Figure B: Chip + Heat Spreader (TAB)

Figure C: Chip + Heat Spreader (TAB) + Capacitors

- Chip Width and Length vary depending on product dimensions

- Each Parameter has its own respective tolerance that is shown throughout the data sheet

- Figures B and C have the same Width (X_{TAB})

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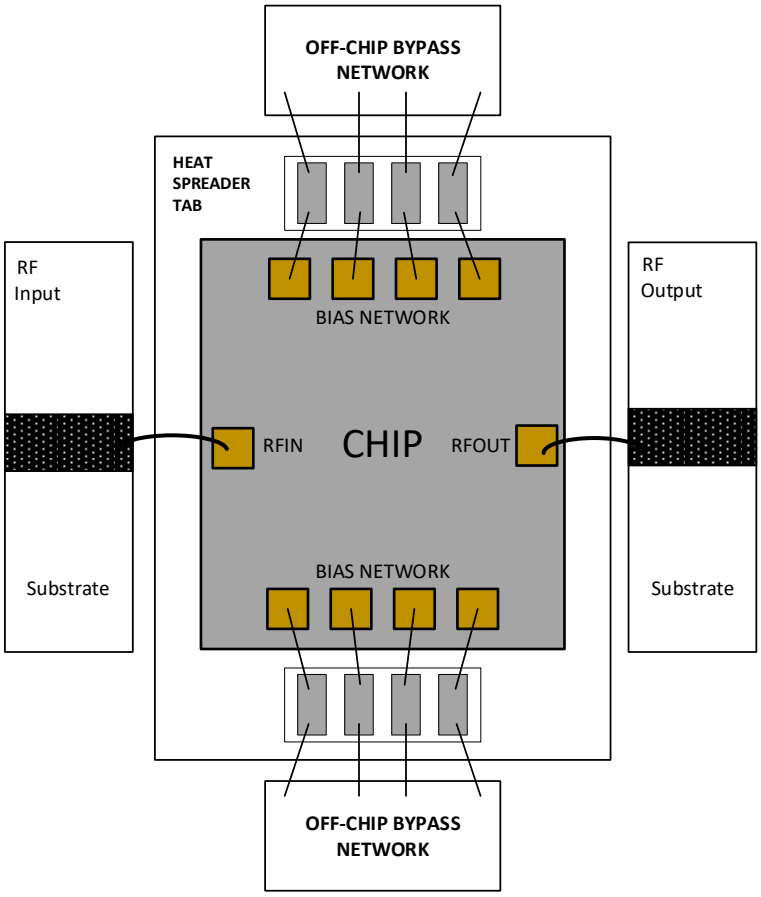
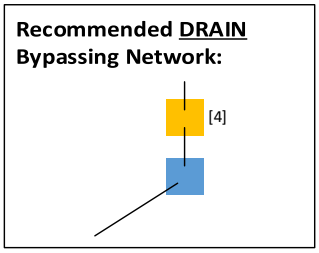
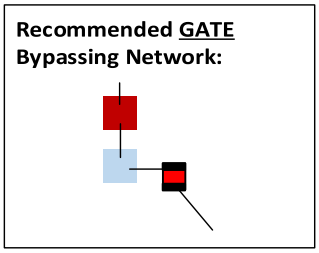
GENERAL BONDING ARRANGEMENT FOR FIGURE C

** BELOW LAYOUT SHOWS BONDING ARRANGEMENT OF A GENERIC AMPLIFIER FOR REFERENCE

** SPECIFIC BYPASS INTERCONNECTIONS DRIVEN BY RESPECTIVE CHIP







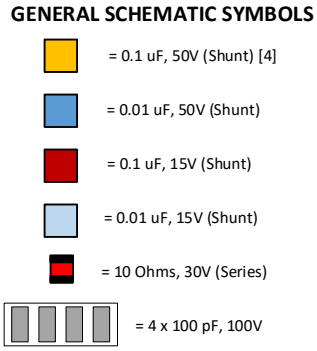


DIAGRAM NOTES

- The 100 pF (15V & 50V) capacitors shown in the "SUGGESTED BONDING ARANGEMENT" Bare Die diagram are replaced with 100 pF (100V) Bar Capacitors for the Capacitor TAB configuration

- The remaining capacitors/resistors previously shown in "SUGGESTED BONDING ARANGEMENT" are the same and now connect to the Bar Capacitors

- Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.

- [4] The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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