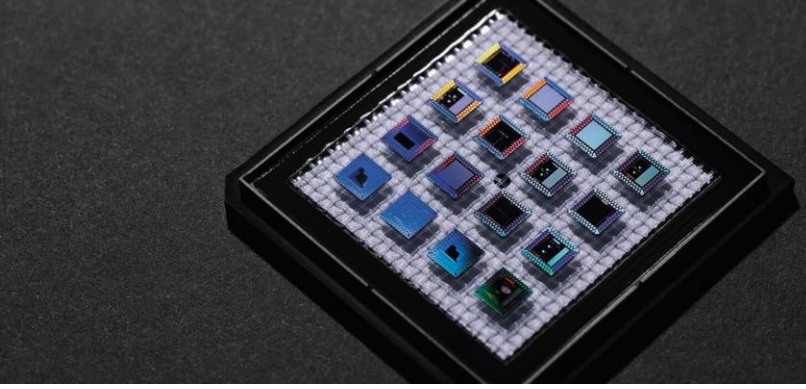
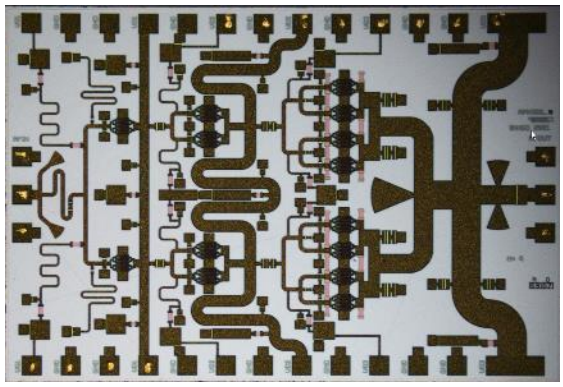


APN352
47 — 51 GHz
GaN Power Amplifier

PRODUCT DESCRIPTION

The APN352 GaN HEMT Power/Driver amplifier is a three-stage Single-ended power device, designed for use in 5G wireless and SatCom Terminals. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.



X= 2.95 mm; Y= 2.00 mm

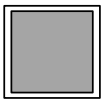
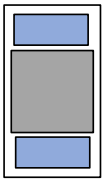
APPLICATIONS

- 5G Wireless
- Internet of Things (IoT)
- SatCom Terminals

PRODUCT FEATURES

- RF frequency: 47.2 to 51.4 GHz
- Linear Gain: 12-16 dB across the band
- Psat: 10 Watt on wafer
- Die Size: 6.4 mm2
- 0.15um GaN HEMT Process
- 3 mil SiC substrate
- DC Power: 28 VDC @ 1.62 A

PRODUCT OPTIONS

OPTION	FIGURE	PART #
BARE DIE		APN352
BARE DIE + TAB		APN352TAB
BARE DIE + TAB + CAPACITORS		APN352TABC

EXPORT INFORMATION

ECCN: 5A991.g

HTS (Schedule B) code: 8542.33.0001

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GaN Power Amplifier

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Drain Voltage	28	V
Gate Voltage Range	-8 to 0	V
Drain Current	2100	mA
Gate Current	0.84	mA
Soldering Temperature	320	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Unit
Drain Voltage Range	20 - 26	V
Gate Voltage Range	-5 to -3	V
Stg 1 Drain Current (Idq)	200	mA
Stg 2 Drain Current (Idq)	528	mA
Stg 3 Drain Current (Idq)	960	mA

ELECTRICAL SPECIFICATIONS

Parameter	Min	Typical	Max	Unit
Operational Frequency	47		51	GHz
Small Signal at 28V				
Small Signal Linear Gain	14		22	dB
Input Return Loss	-9		-4	dB
Output Return Loss	-32		-7	dB
On-Wafer Pulsed Power at 28V				
Psat (at 25 dBm)	39.2	40.5	41.8	dBm
Power Gain (at 25 dBm)	14.3	15.5	16.8	dB
P1db	38	40	42	dBm
PAE (at 25 dBm)	11.5	20.3	22	%
Max PAE	13.2	20.7	22.5	%
Fixtured CW at 20V, 25°C Case Temp				
Psat (at 25 dBm)	36.9	37.4	38.5	dBm
Power Gain (at 25 dBm)	11.9	12.4	13.5	dB
PAE (at 25 dBm)	9.3	11.4	14.2	%
Max PAE	3.8	11.8	14.2	%
Drain Voltage		26		V
Stage 1 Gate Voltage		-4.155		V
Stage 2 Gate Voltage		-4.155		V
Stage 1 Idq		200		mA
Stage 2 Idq		528		mA

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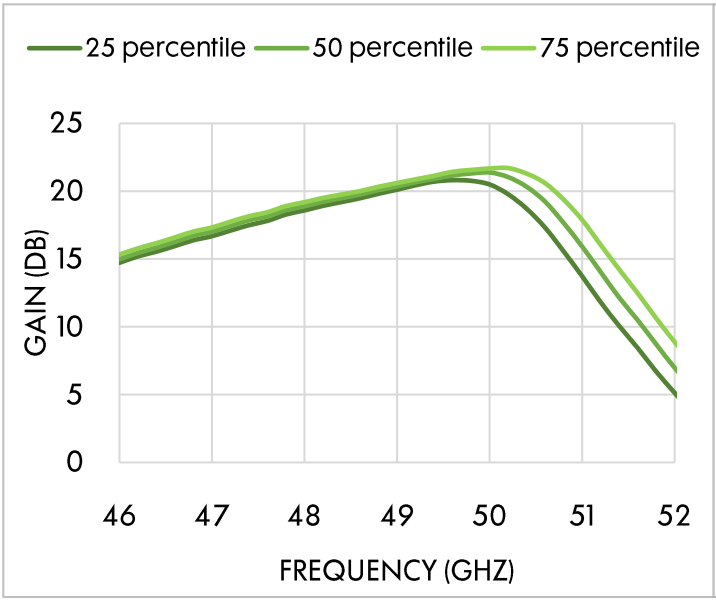
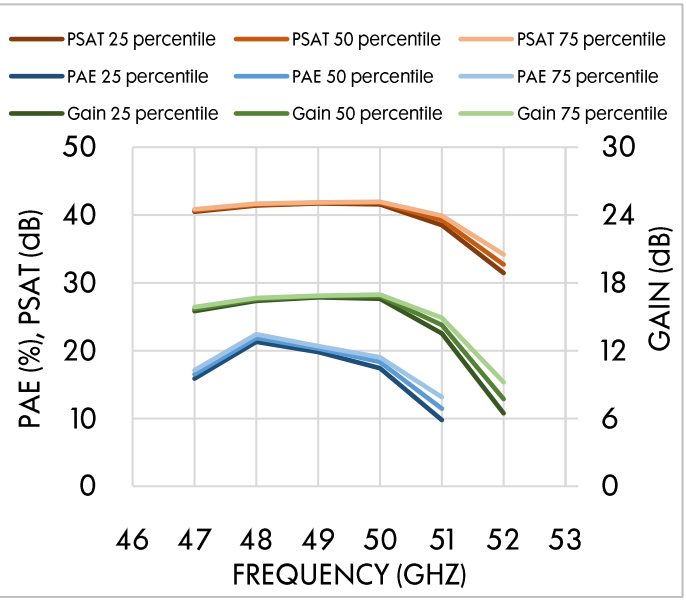
Pulsed On wafer measured Performance Characteristics (Typical Performance at 25°C)

Vd= 28.0 V, Id1+Id1a = 520 mA, Id2+Id2a = 2100 mA. *

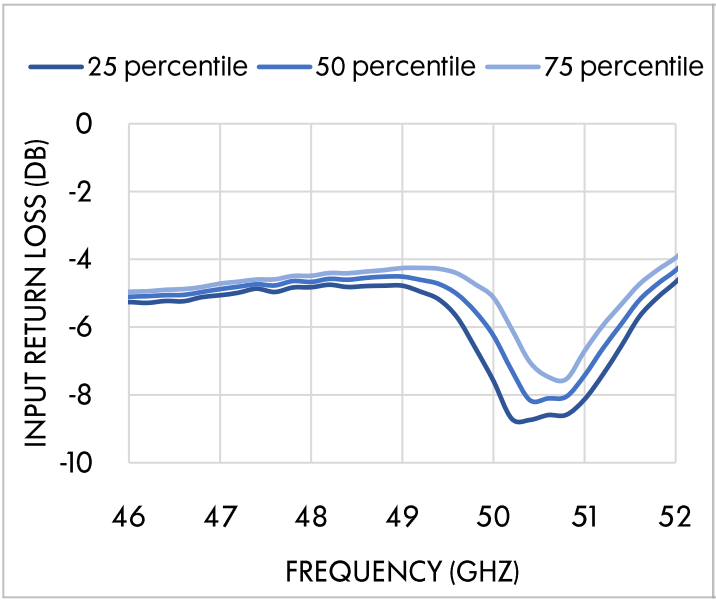
Small Signal Gain vs. Frequency



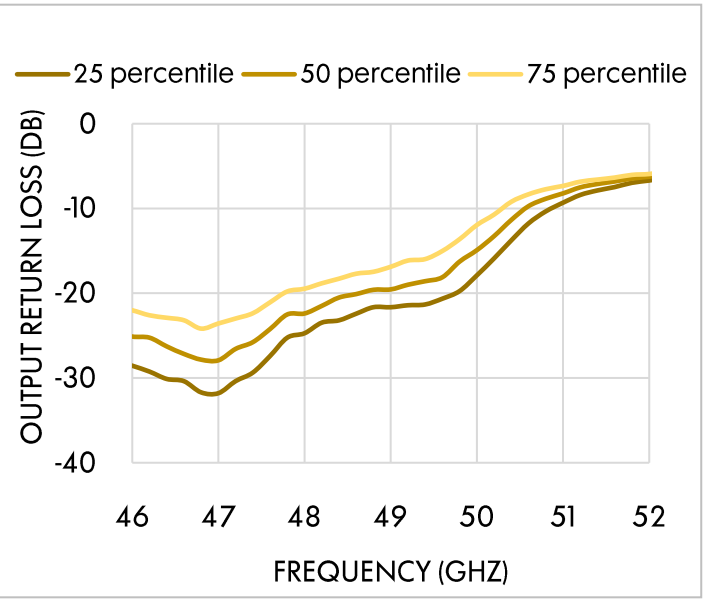
Large Signal PAE, Gain, PSAT vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



* Pulsed-power on-wafer

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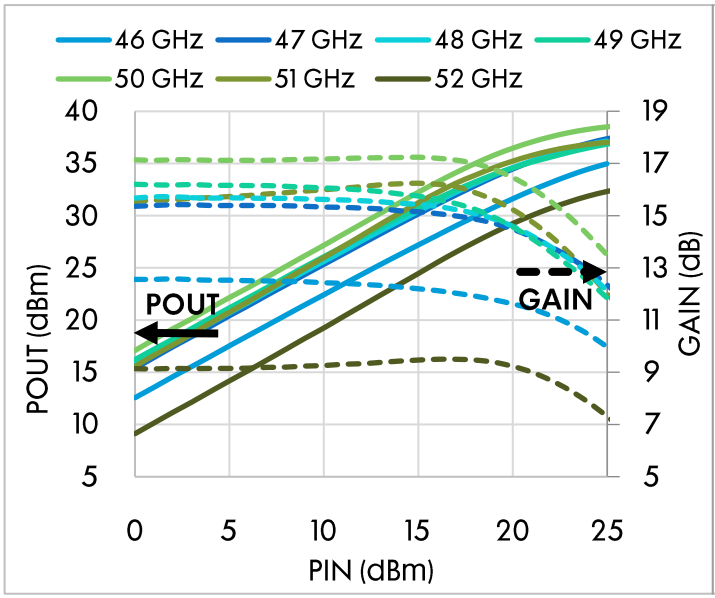
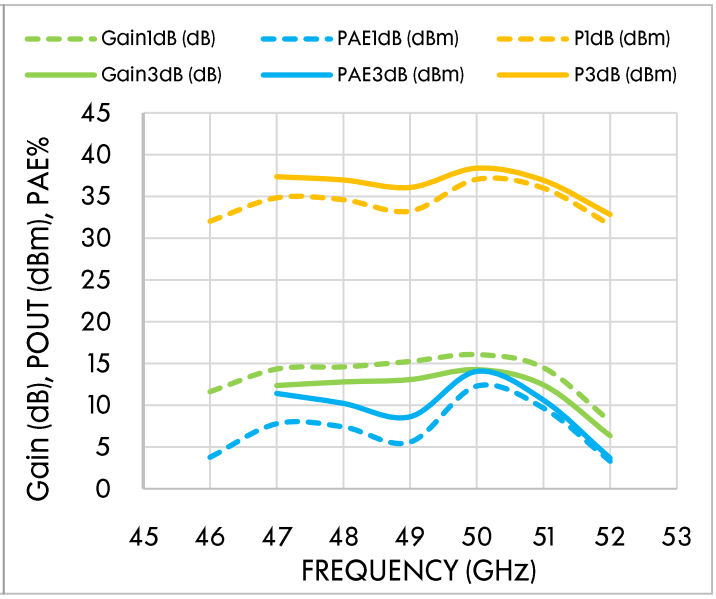
Fixture measured Performance Characteristics (Typical Performance at 25°C)

Vd = 20.0 V, Id1 = 520 mA, Id2 =2100 mA

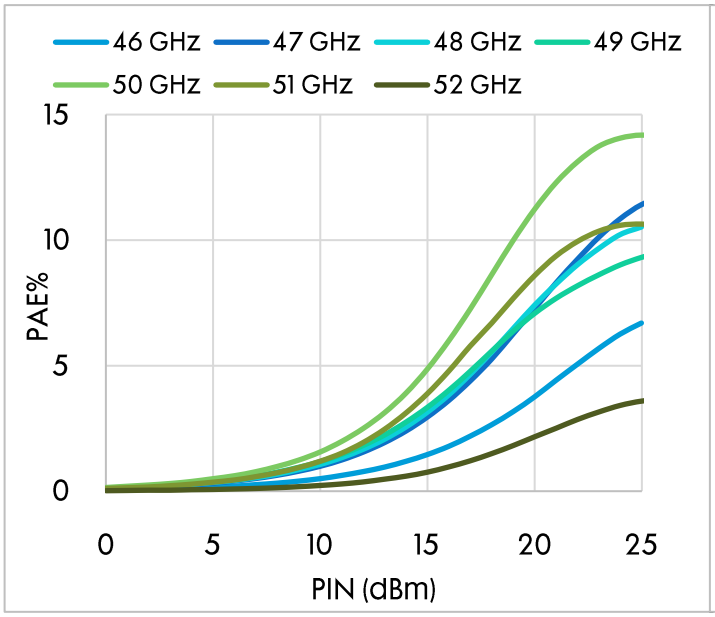
POUT and Gain vs. PIN



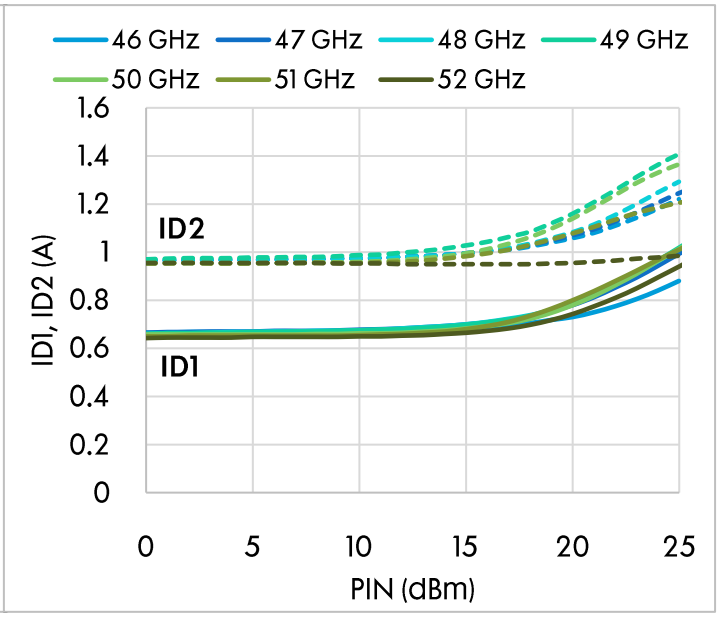
PAE, Gain, POUT vs. Frequency



PAE vs. PIN



ID1, ID2 vs. PIN



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DIE SIZE AND BOND PAD LOCATIONS

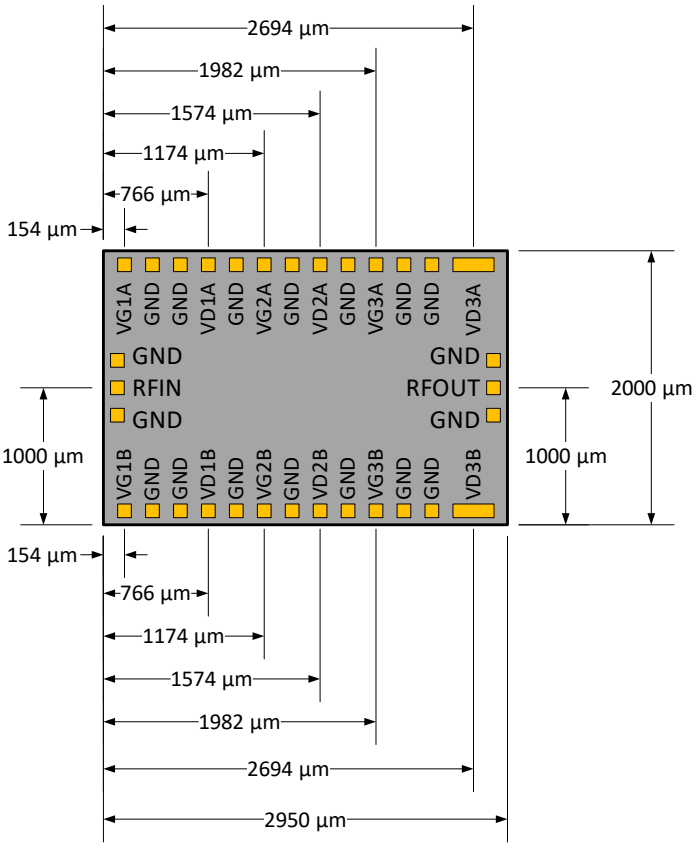
X =2950 µm ± 25 µm

Y = 2000 ± 25 µm

DC Bond Pad = 100 x 100 ± 0.5 µm

RF Bond Pad = 100 x 100 ± 0.5 µm

Chip Thickness = 75 ± 5 µm



BIASING/DE-BIASING DETAILS:

Bias for 1st stage is from top.

The 2nd stages must bias up from both sides.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limited positive gate bias (G-S or G-D) to < 1V

b. Know your devices' breakdown voltages

c. Use a power supply with both voltage and current limit

d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture
    a. Apply negative gate voltage (-8 V) to ensure that all devices are off
    b. Ramp up drain bias to ~10 V
    c. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    d. Ramp up drain to operating bias
    e. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved

e. To safely de-bias GaN devices, start by de-biasing output amplifier stages first (if applicable):
    a. Set gate voltage back to pinch-off (-8 V)
    b. Gradually decrease drain bias to 0 V
    c. Gradually decrease gate bias to 0 V
    d. Turn off supply voltages

f. Repeat de-bias procedure for each amplifier stage

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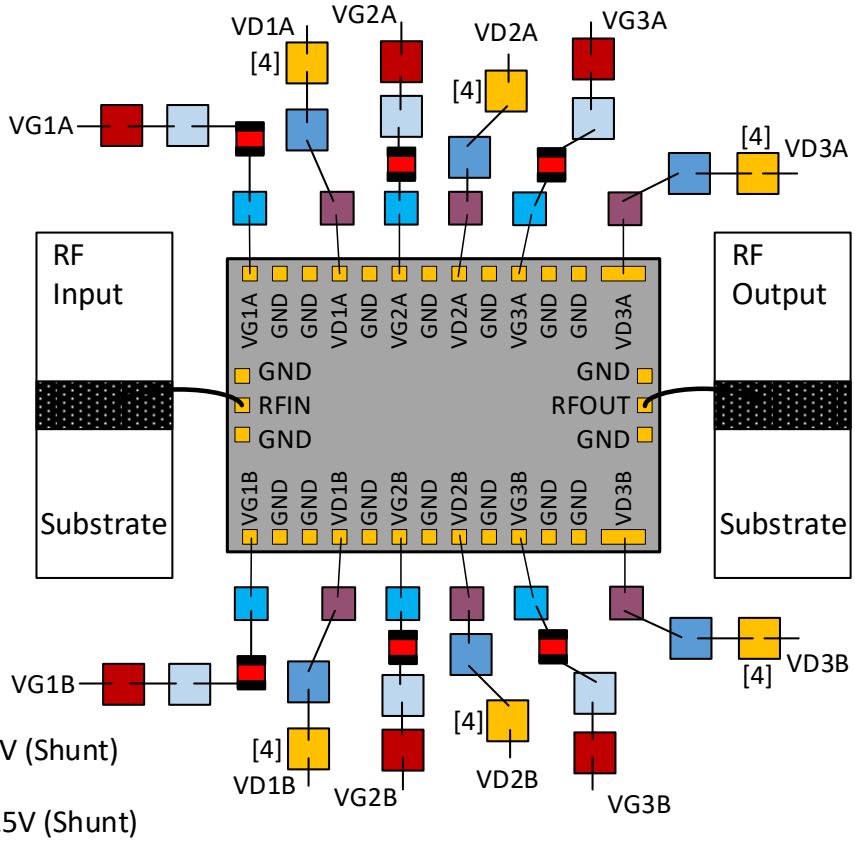
RECOMMENDED ASSEMBLY NOTES

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

SUGGESTED BONDING ARRANGEMENT



GENERAL DIAGRAM SYMBOLS

= 0.1 uF, 50V (Shunt) [4]

= 0.1 uF, 15V (Shunt)

= 0.01 uF, 50V (Shunt)

= 0.01 uF, 15V (Shunt)

= 100 pF, 50V (Shunt)

= 100 pF, 15V (Shunt)

= 10 Ohms, 30V (Series)

MOUNTING PROCESSES

Most NGSS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGSS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320 °C for 30 seconds.

Note: Many of the NGSS parts do incorporate airbridges, so caution should be used when determining the pickup tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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