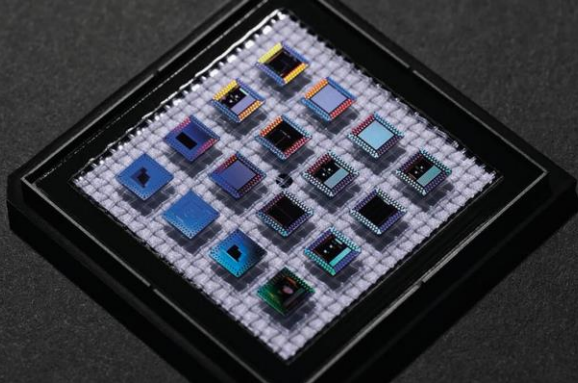




APN228

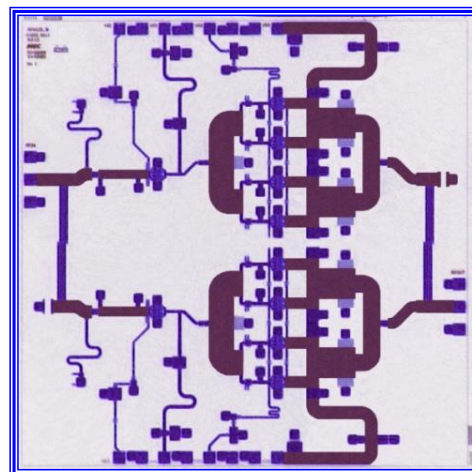
27 – 31 GHz

GaN Power Amplifier

*** PLEASE REFER TO GENERAL CHIP DIAGRAMS FOR TAB DIMENSIONING AND BONDING ***

PRODUCT DESCRIPTION

The APN228 monolithic GaN HEMT amplifier is a broadband, two-stage power device, designed for use in SatCom Terminals and point-to-point digital radios. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.



X= 4.0 mm; Y= 4.0 mm

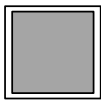
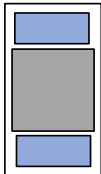
APPLICATIONS

- Point-to-Point Digital Radios
- Point-to-Multipoint Digital Radios
- SatCom Terminals

PRODUCT FEATURES

- RF frequency: 27 to 31 GHz
- Linear Gain: 16 dB typ.
- Psat: ~16 W on wafer, typical
- Psat: ~12.5 W (CW)
- Die Size: 16 sq. mm.
- 0.2um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 28 VDC @ 1.2 A

PRODUCT OPTIONS

OPTION	FIGURE	PART #
BARE DIE		APN228
BARE DIE + TAB		APN228TAB
BARE DIE + TAB + CAPACITORS		APN228TABC

EXPORT INFORMATION

ECCN: 3A001.b.2.c

HTS (Schedule B) code: 8542.33.0001



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APN228

27 – 31 GHz

GaN Power Amplifier

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Drain Voltage	28	V
Gate Voltage Range	-8 to 0	V
Drain Current	1500	mA
Gate Current	0.6	mA
Power Dissipation*	42	W
Soldering Temperature	320	°C

*7W/mm of gate periphery

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Unit
Drain Voltage Range	20 - 28	V
Gate Voltage Range	-5 to -3	V
Stg 1 Drain Current (Idq)	240	mA
Stg 2 Drain Current (Idq)	240 - 960	mA

ELECTRICAL SPECIFICATIONS

Parameter	Min	Typical	Max	Unit
Operational Frequency	27		31	GHz
Small Signal at 28V				
Small Signal Linear Gain	18		19	dB
Input Return Loss	-35.5		-17	dB
Output Return Loss	-20		-15	dB
On-Wafer Pulsed Power at 28V				
Psat (at 26 dBm)	41.7	42	42.8	dBm
Power Gain (at 26 dBm)	15.7	16.2	17	dB
PIdb	42	42.6	43	dBm
PAE (at 26 dBm)	32.2	33	36.7	%
Max PAE	33	34	37.2	%
Fixtured CW at 28V, 25°C Case Temp				
Psat (at 26 dBm)	41	41.6	42	dBm
Power Gain (at 26 dBm)	15	15.6	16	dB
PAE (at 26 dBm)	27.2	28	30.3	%
Max PAE	28		31	%
Drain Voltage		28		V
Stage 1 Gate Voltage		-4.370		V
Stage 2 Gate Voltage		-4.320		V
Stage 1 Idq		240		mA
Stage 2 Idq		960		mA

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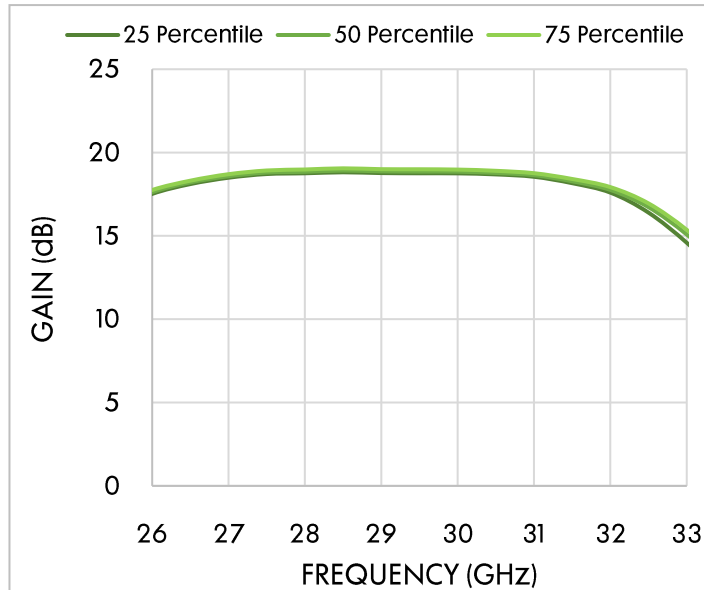
27 – 31 GHz

GaN Power Amplifier

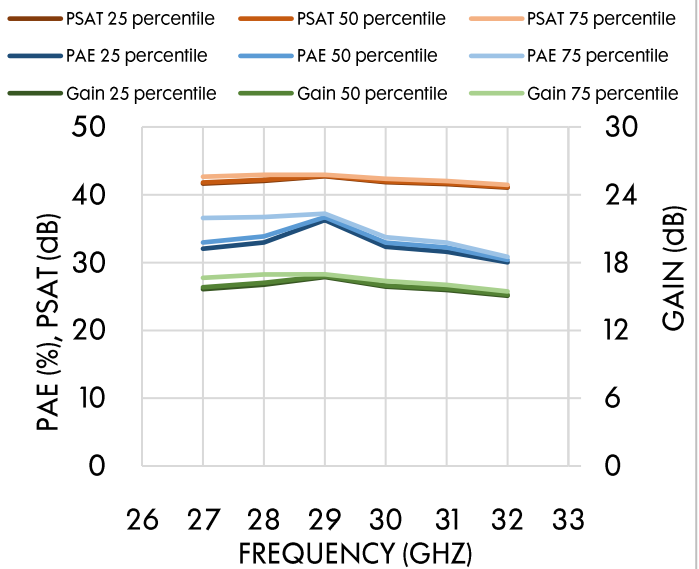
Pulsed On wafer measured Performance Characteristics (Typical Performance at 25°C)

$V_d = 28.0\text{ V}$, $I_{d1} + I_{d1a} = 240\text{ mA}$, $I_{d2} + I_{d2a} = 960\text{ mA}$. *

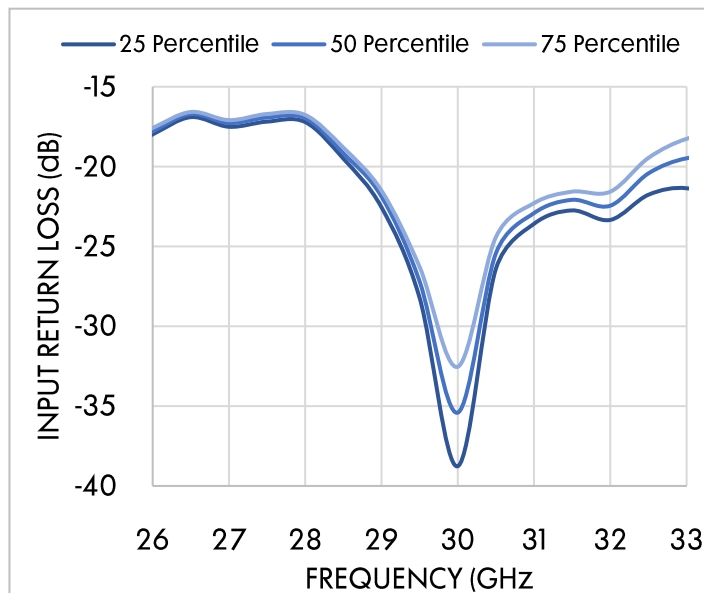
Small Signal Gain vs. Frequency



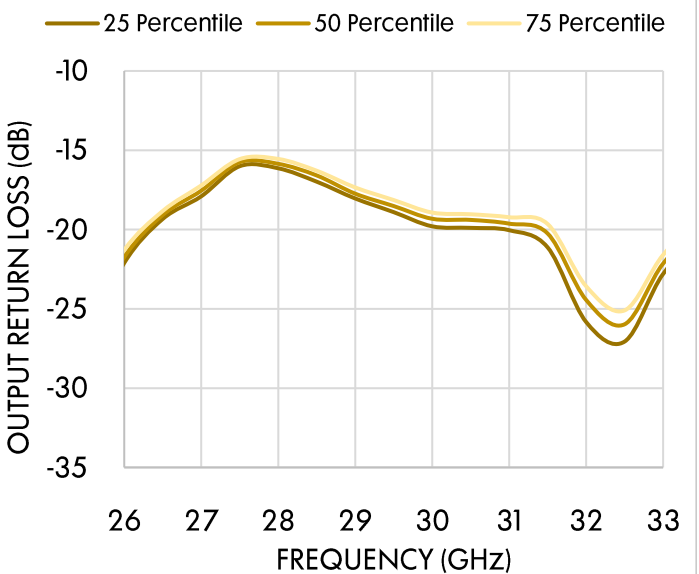
Large Signal PAE, Gain, PSAT vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



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* Pulsed-power on-wafer

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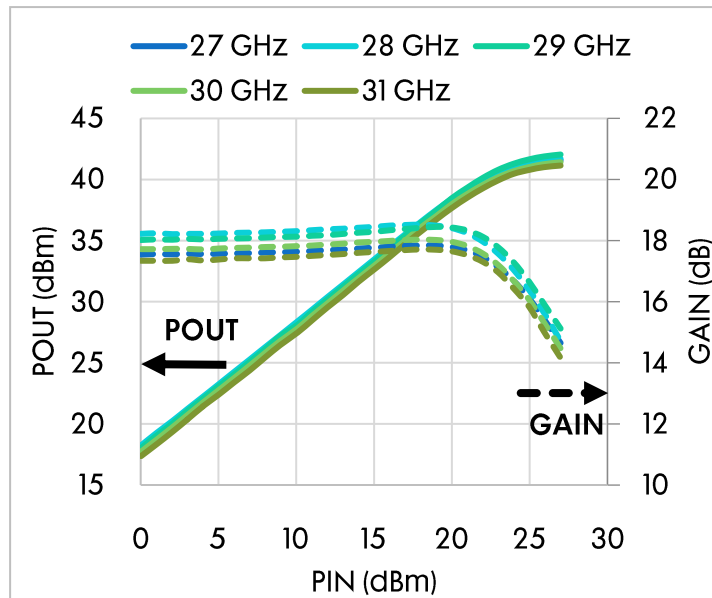
27 – 31 GHz

GaN Power Amplifier

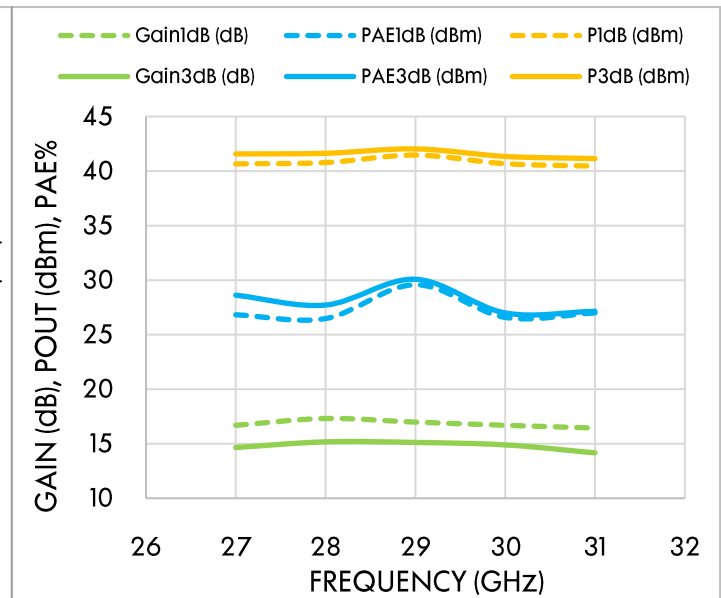
Fixture measured Performance Characteristics (Typical Performance at 25°C)

$V_d = 28.0\text{ V}$, $I_{d1} = 240\text{ mA}$, $I_{d2} = 960\text{ mA}$

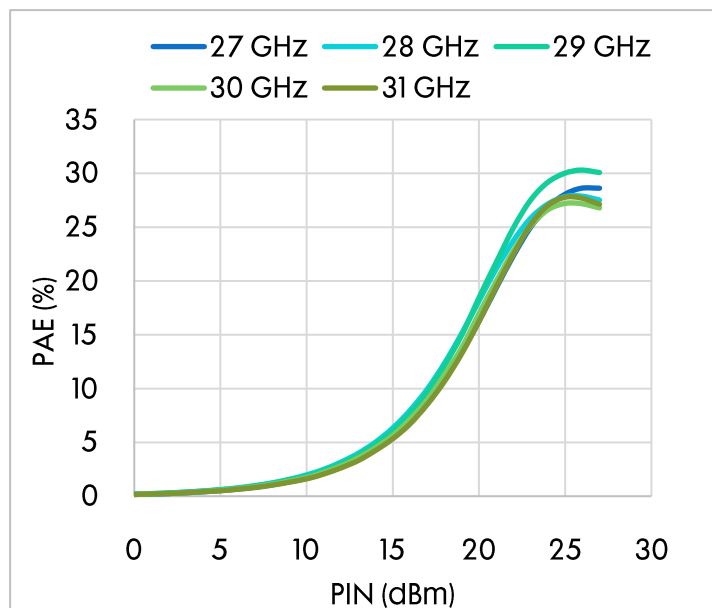
POUT and Gain vs. PIN



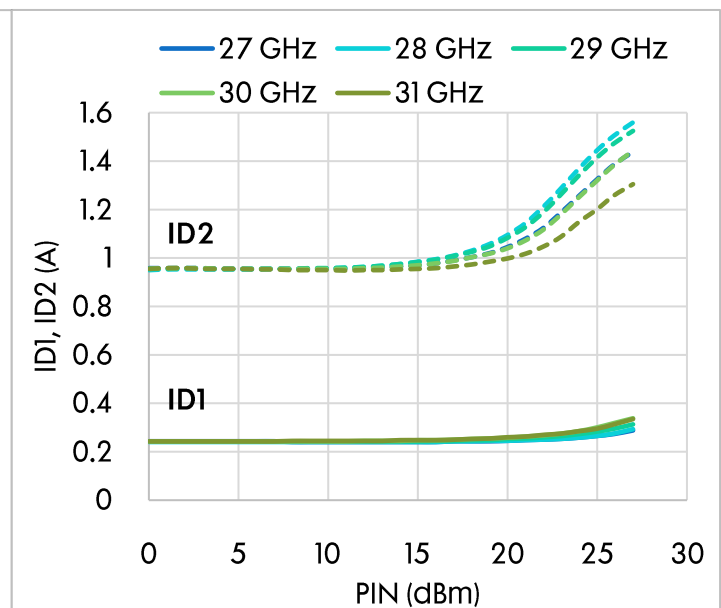
PAE, Gain, POUT vs. Frequency



PAE vs. PIN



ID1, ID2 vs. PIN



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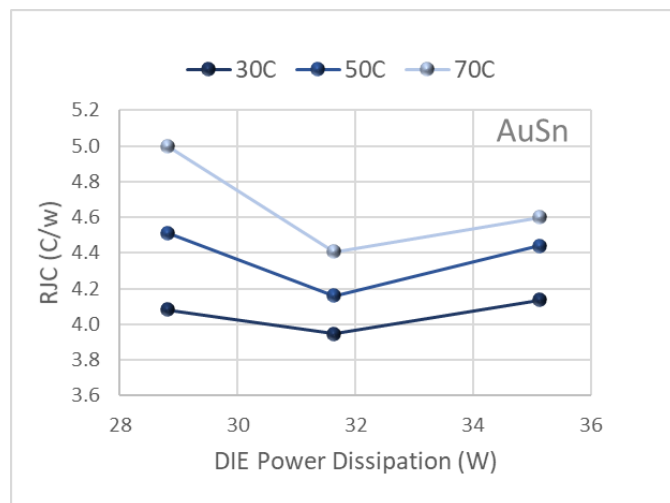
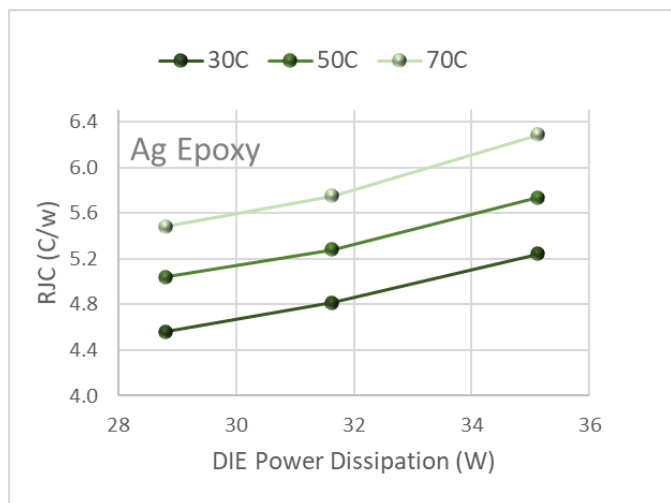
APN228

27 – 31 GHz

GaN Power Amplifier

Preliminary Thermal Properties with die mounted with 25 um 80/20 AuSn Eutectic ** to: 10 mil CuW10 Shim

Shim	Mounting Material	Average Backside Die Temperature	Hottest Junction Temperature T _{jc}	RF Output (dBm)	Power Dissipation (W)	Thermal Resistance R _{jc} (°C/W)
10 mil CuW	AuSn Eutectic	30 °C	147	39.8	28.8	4.1
			155	41.0	31.6	4.0
			175	41.3	35.1	4.1
		50 °C	180	39.8	28.8	4.5
			181	41.0	31.6	4.2
			206	41.3	35.1	4.4
		70 °C	213	39.8	28.8	5.0
			209	41.0	31.6	4.4
			218	41.3	35.1	4.2
10 mil CuW	Silver Epoxy	30 °C	161	39.8	28.8	4.6
			182	41.0	31.6	4.8
			214	41.3	35.1	5.2
		50 °C	195	39.8	28.8	5.0
			217	41.0	31.6	5.3
			251	41.3	35.1	5.7
		70 °C	228	39.8	28.8	5.5
			252	41.0	31.6	5.8
			291	41.3	35.1	6.3



** V_d = 28.0 V, I_{dq} = 240 mA, I_{d2q} = 960 mA

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27 – 31 GHz

GaN Power Amplifier

DIE SIZE AND BOND PAD LOCATIONS

X = 4000 μm $\pm$ 25 μm

Y = 4000 $\pm$ 25 μm

DC Bond Pad = 100 x 100 $\pm$ 0.5 μm

RF Bond Pad = 100 x 100 $\pm$ 0.5 μm

Chip Thickness = 101 $\pm$ 5 μm

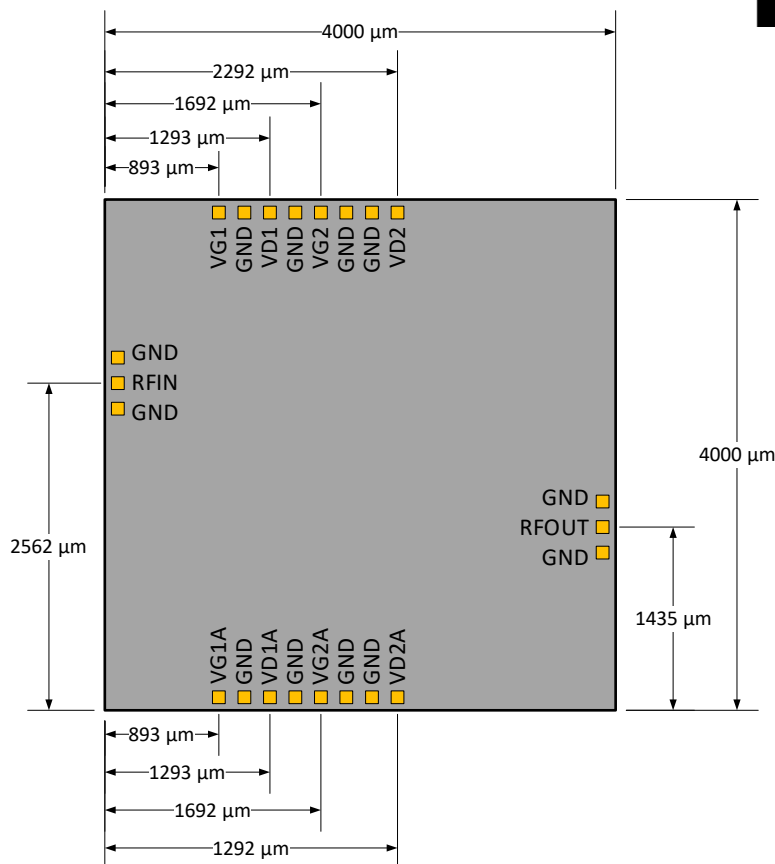
BIASING/DE-BIASING DETAILS:

Bias for 1st stage is from top.

The 2nd stages must bias up from both sides.

Listed below are some guidelines for GaN device testing and wire bonding:

- Limited positive gate bias (G-S or G-D) to < 1V
- Know your devices' breakdown voltages
- Use a power supply with both voltage and current limit
- With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture
 - Apply negative gate voltage (-8 V) to ensure that all devices are off
 - Ramp up drain bias to ~10 V
 - Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
 - Ramp up drain to operating bias
 - Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
- To safely de-bias GaN devices, start by de-biasing output amplifier stages first (if applicable):
 - Set gate voltage back to pinch-off (-8 V)
 - Gradually decrease drain bias to 0 V
 - Gradually decrease gate bias to 0 V
 - Turn off supply voltages
- Repeat de-bias procedure for each amplifier stage



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APN228

27 – 31 GHz

GaN Power Amplifier

TAB-DIE SIZE AND BOND PAD LOCATIONS

CuMoCu-based Tab

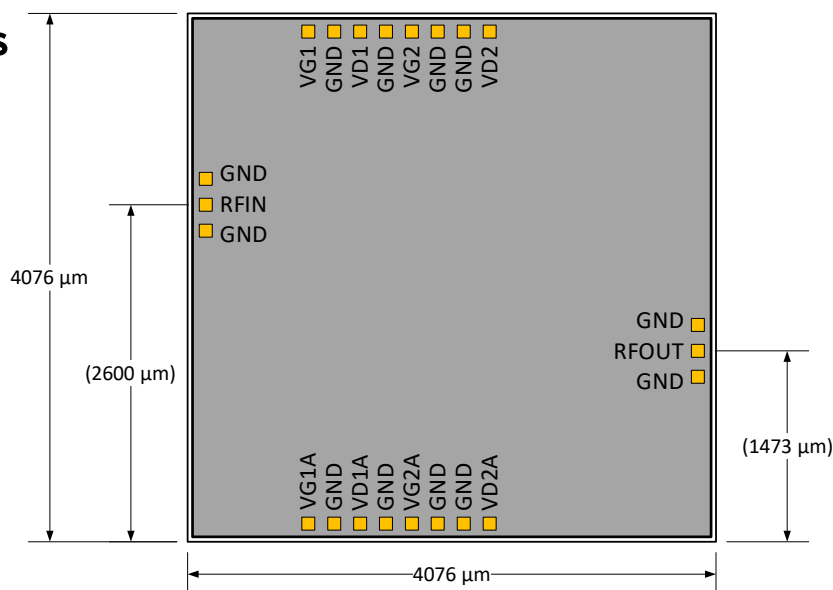
$X = 4076 \mu\text{m} \pm 25 \mu\text{m}$

$Y = 4076 \mu\text{m} \pm 25 \mu\text{m}$

Tab Thickness = $254 \mu\text{m} \pm 25 \mu\text{m}$

Eutectic Solder layer

Eutectic Thickness = 1 mil ($25 \mu\text{m}$) nominal



APN228TAB

TAB-CAPACITOR-DIE SIZE AND BOND PAD LOCATIONS

CuMoCu-based Tab + Capacitors

$X = 4076 \mu\text{m} \pm 25 \mu\text{m}$

$Y = 5775 \mu\text{m} \pm 25 \mu\text{m}$

Tab Thickness = $254 \mu\text{m} \pm 25 \mu\text{m}$

Eutectic Solder layer

Eutectic Thickness = 1 mil ($25 \mu\text{m}$) nominal

100pF, 100V Bar Capacitors

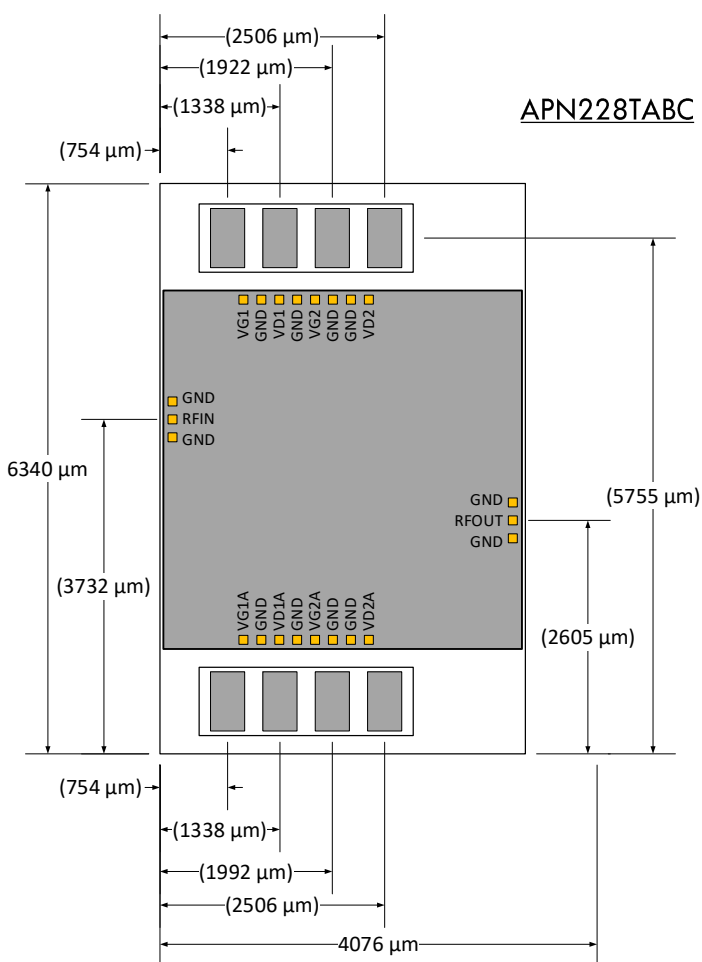
$X = 2388 \mu\text{m} \pm 76 \mu\text{m}$

$Y = 762 \mu\text{m} \pm 76 \mu\text{m}$

DC Gold Bond Pad = $381 \times 660 \mu\text{m}$ nominal

Cap Thickness = $127 \mu\text{m} \pm 38 \mu\text{m}$

Cap Part Number = CRM-BN-94X30X5-G-101-Z-CE396 (or equivalent)



APN228TABC

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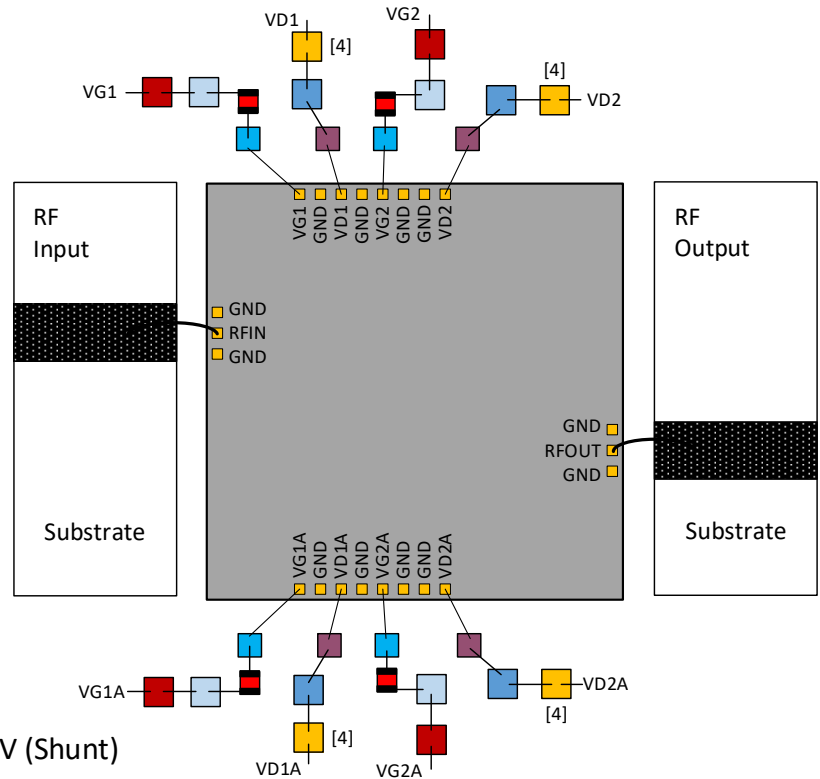
27 – 31 GHz

GaN Power Amplifier

RECOMMENDED ASSEMBLY NOTES

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF, 50V Capacitors.

SUGGESTED BONDING ARRANGEMENT



GENERAL DIAGRAM SYMBOLS

	= 0.1 uF, 50V (Shunt) [4]		= 0.1 uF, 15V (Shunt)
	= 0.01 uF, 50V (Shunt)		= 0.01 uF, 15V (Shunt)
	= 100 pF, 50V (Shunt)		= 100 pF, 15V (Shunt)
	= 10 Ohms, 30V (Series)		

MOUNTING PROCESSES

Most NGSS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGSS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320 °C for 30 seconds.

Note: Many of the NGSS parts do incorporate airbridges, so caution should be used when determining the pickup tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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27 – 31 GHz

GaN Power Amplifier

GENERAL CHIP DIAGRAM FOR DIMENSIONING

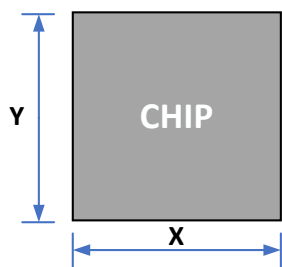


Figure A

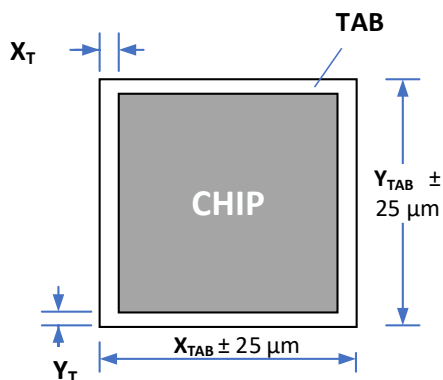


Figure B

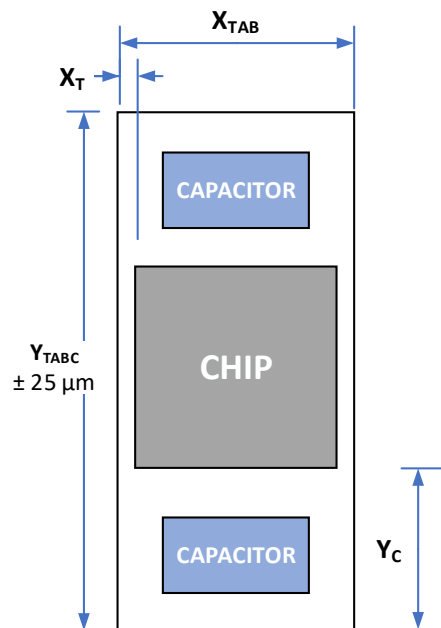


Figure C

SCHEMATIC LEGEND

Parameter	Value	Tolerance
Chip Width (X)	See Die Size Page	See Die Size Page
Chip Length (Y)	See Die Size Page	See Die Size Page
Tab-Chip Width Offset (X_T)	$38 \mu m$ (0.0015")	-
Tab-Chip Length Offset (Y_T)	$38 \mu m$ (0.0015")	-
TAB Width (X_{TAB})	$X_{TAB} = X + 76 \mu m$	$\pm 25 \mu m$
TAB Length (Y_{TAB})	$Y_{TAB} = Y + 76 \mu m$	$\pm 25 \mu m$
Chip Edge to TAB Edge Length (Y_C)	$1170 \mu m$ (0.046")	-
Tab-Chip-Capacitor Length (Y_{TAB_C})	$Y_{TAB_C} = Y + 2 \cdot Y_C$	$\pm 25 \mu m$

NOTES

Figure A: Chip

Figure B: Chip + Heat Spreader (TAB)

Figure C: Chip + Heat Spreader (TAB) + Capacitors

- Chip Width and Length vary depending on product dimensions

- Each Parameter has its own respective tolerance that is shown throughout the data sheet

- Figures B and C have the same Width (X_{TAB})

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27 – 31 GHz

GaN Power Amplifier

GENERAL BONDING ARRANGEMENT FOR FIGURE C

**** BELOW LAYOUT SHOWS BONDING ARRANGEMENT OF A GENERIC AMPLIFIER FOR REFERENCE**

**** SPECIFIC BYPASS INTERCONNECTIONS DRIVEN BY RESPECTIVE CHIP**

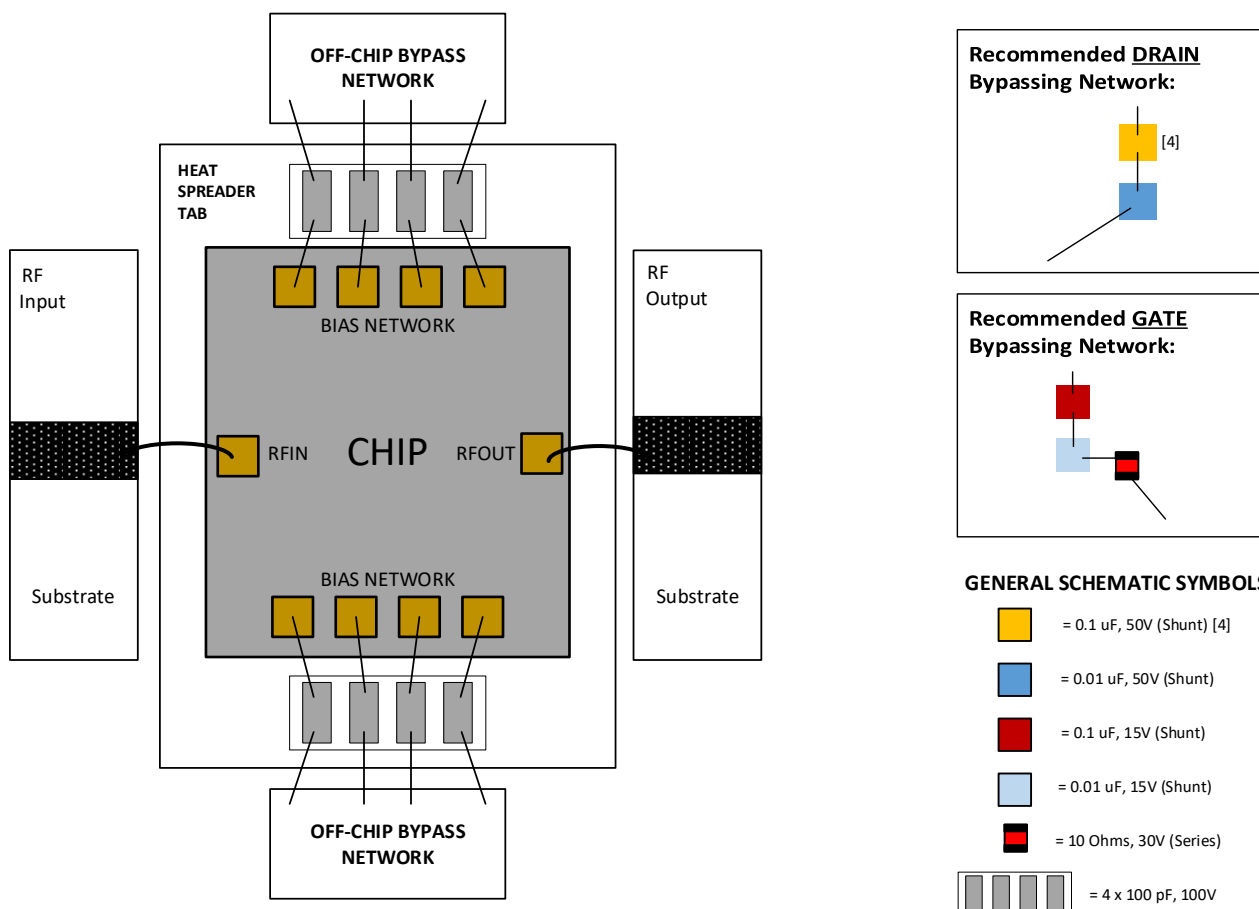


DIAGRAM NOTES

- The 100 pF (15V & 50V) capacitors shown in the “SUGGESTED BONDING ARRANGEMENT” Bare Die diagram are replaced with 100 pF (100V) Bar Capacitors for the Capacitor TAB configuration
- The remaining capacitors/resistors previously shown in “SUGGESTED BONDING ARRANGEMENT” are the same and now connect to the Bar Capacitors
- Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
- [4] The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

PLEASE ALSO REFER TO OUR “GaN Chip Handling Application Note” BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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