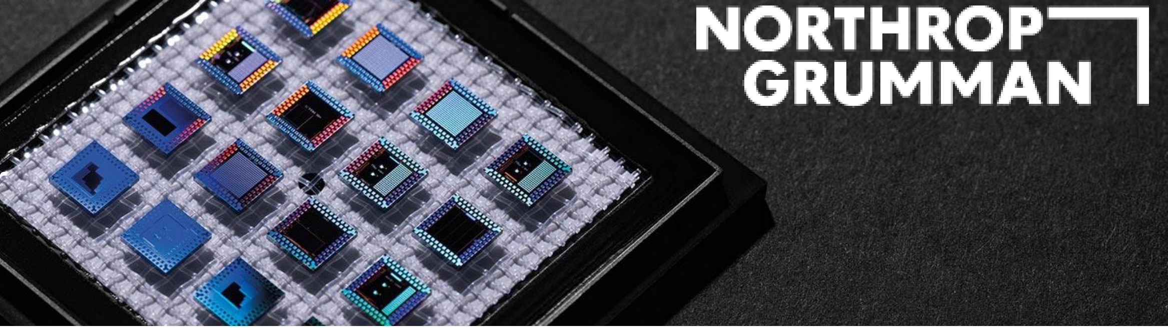
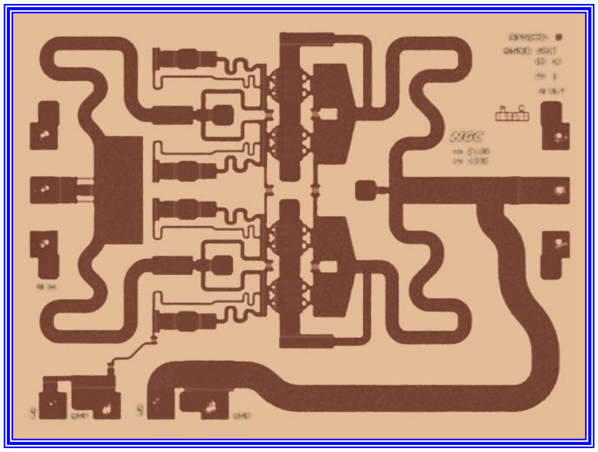
APN232
13.5-15.5 GHz
GaN Power Amplifier





X = 2.1 mm Y = 1.55 mm

Applications

- Point-to-Point Digital Radios
- Point-to-Multipoint Digital Radios
- SATCOM Terminals

Product Description

The APN232 monolithic GaN HEMT amplifier is a broadband, single-stage power device, designed for use in SATCOM Terminals and point-to-point digital radios. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Product Features

- RF frequency: 13.5 to 15.5 GHz
- Linear Gain: 13 dB typ.
- Psat: 42 dBm typ.
- PAE% @ Psat: 43% typ.
- Die Size: 3.255 sq. mm.
- 0.2um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 28 VDC @ 640 mA

Performance Characteristics (Ta = 25°C)

Specification	Min	Typ	Max	Unit
Frequency	13.5		14	GHz
Linear Gain	12	13		dB
Input Return Loss	7	10		dB
Output Return Loss	5	9		dB
P1dB (PP*)		38.5		dBm
Psat (PP*)	38.5	42		dBm
PAE @ Psat (PP*)		43		%
Vd		28		V
Vg		-3.5		V
Id		640		mA

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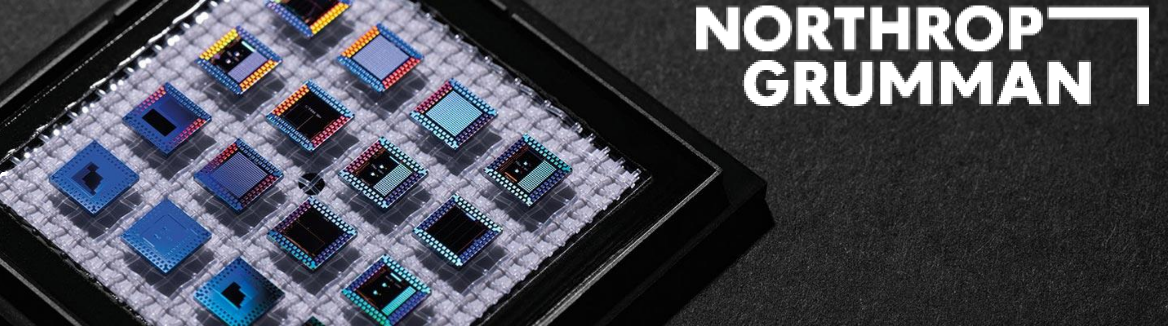

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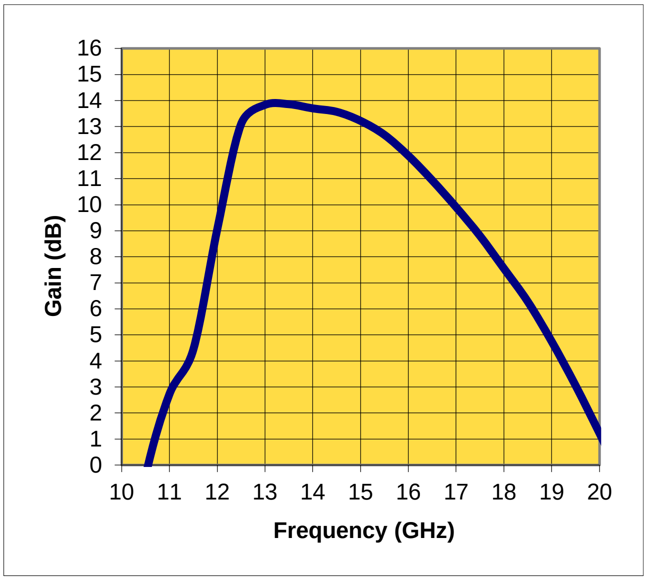
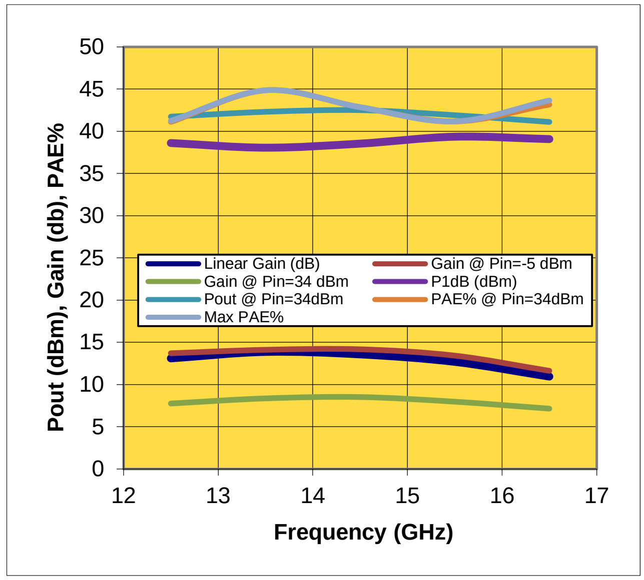
GaN Power Amplifier

On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28 V, Id = 640 mA. *

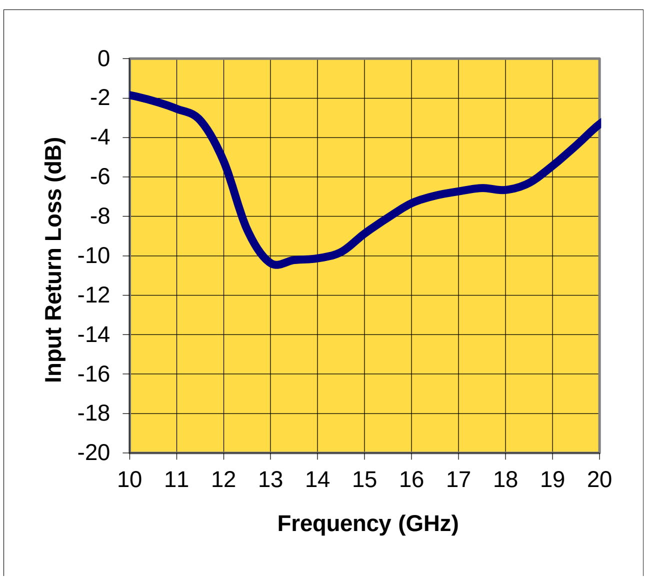
GAIN vs. Frequency



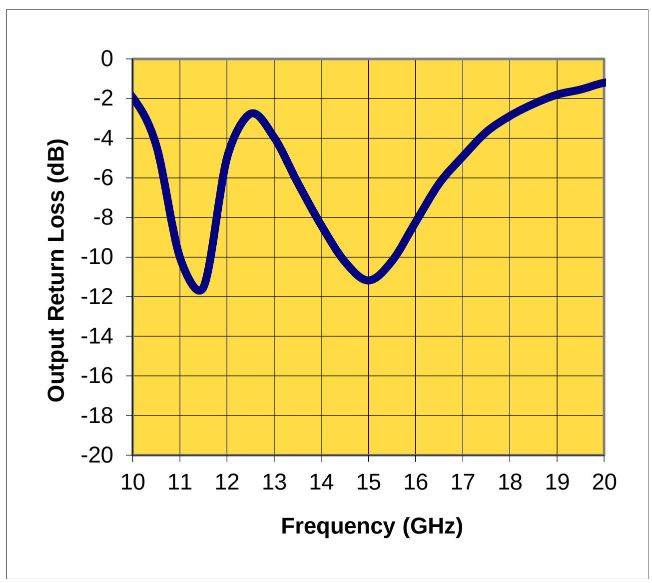
PAE, GAIN, Pout vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



*Pulsed-power on-wafer

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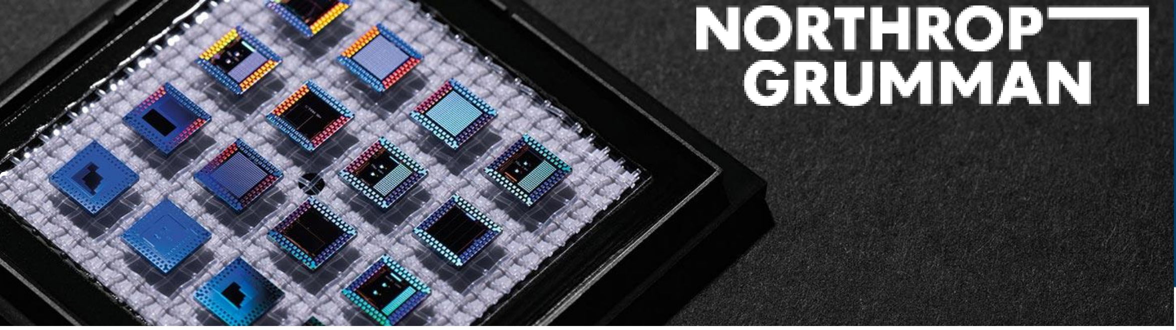

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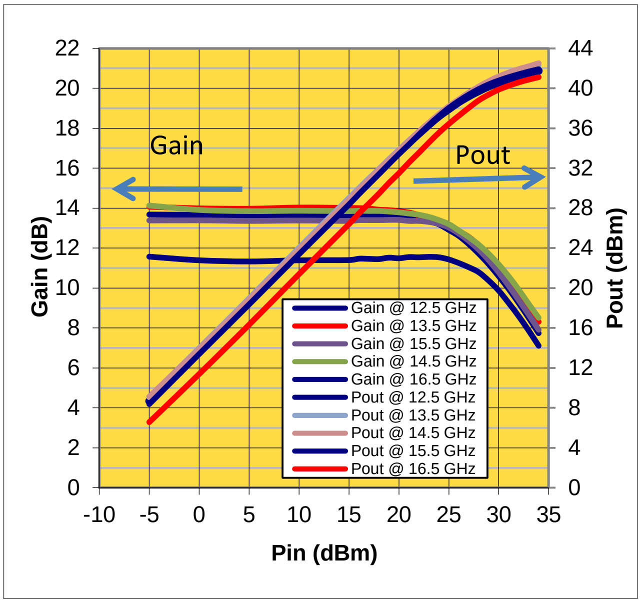
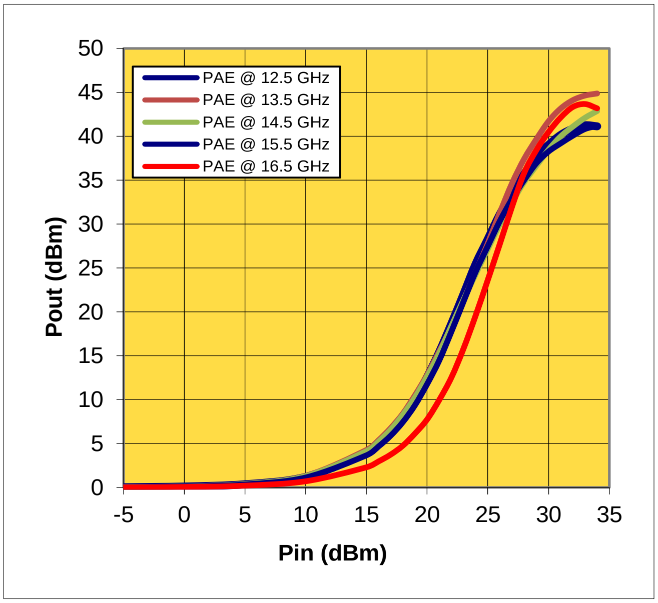
On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28 V, Id = 640 mA. *

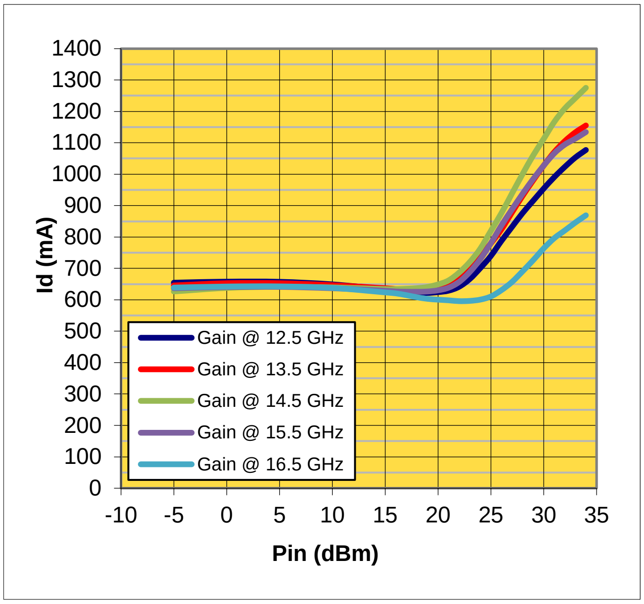
GAIN, Pout vs. Pin



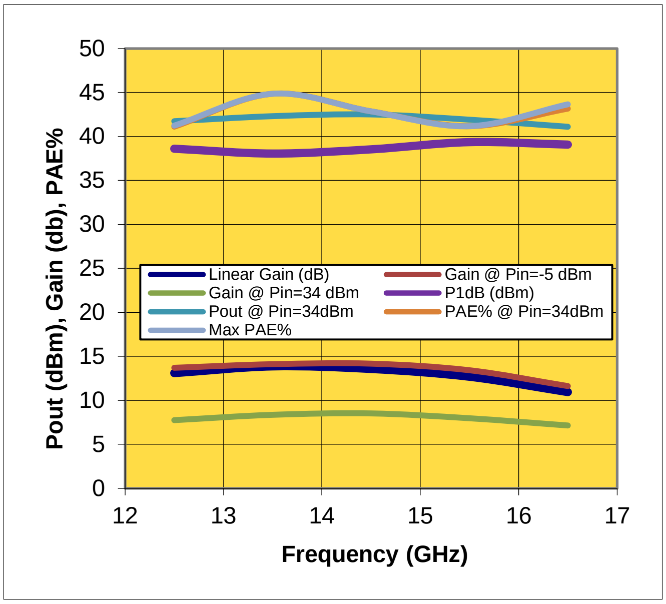
PAE vs. Pin



Id vs Pin



Pout, Gain, PAE vs. Frequency



*Pulsed-power on-wafer

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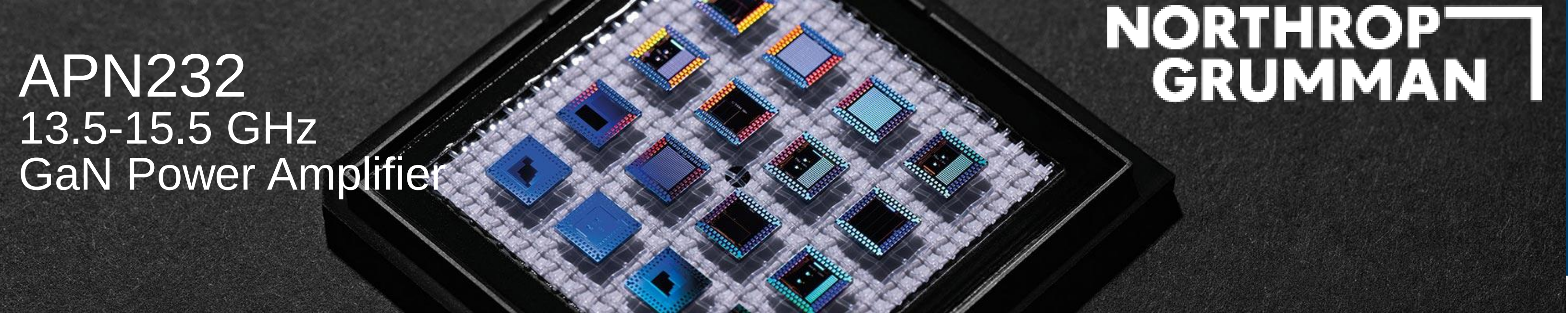

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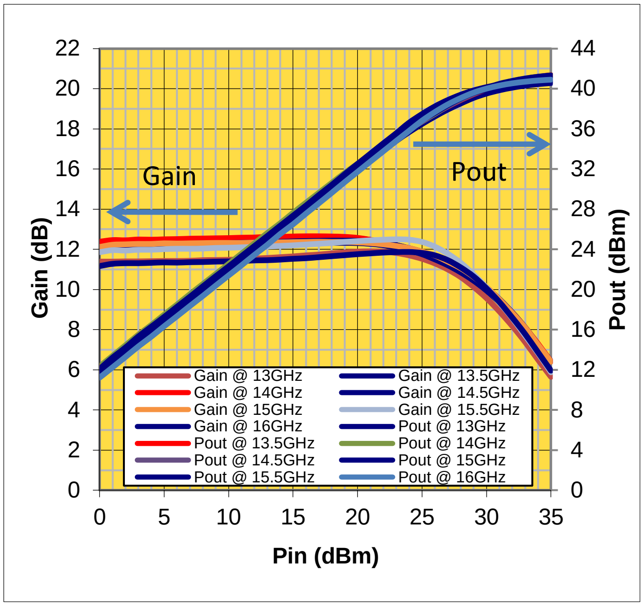
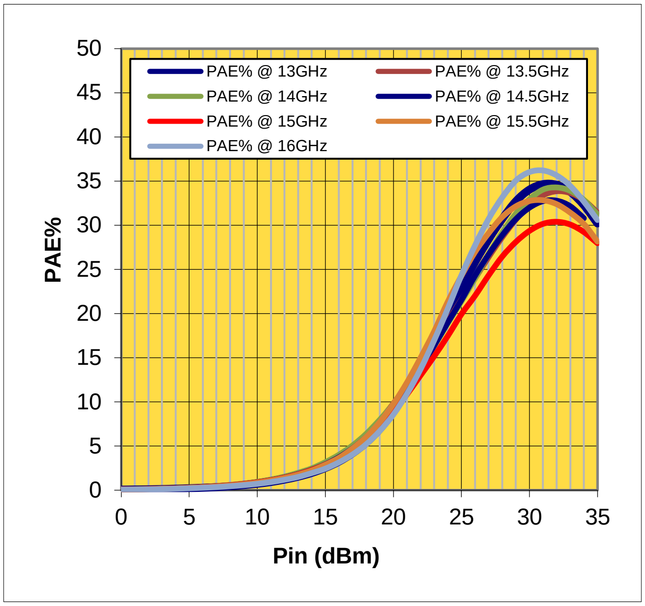
Measured fixture Performance Characteristics (Typical Performance at 25°C)
Vd = 28 V, Id = 640 mA. **

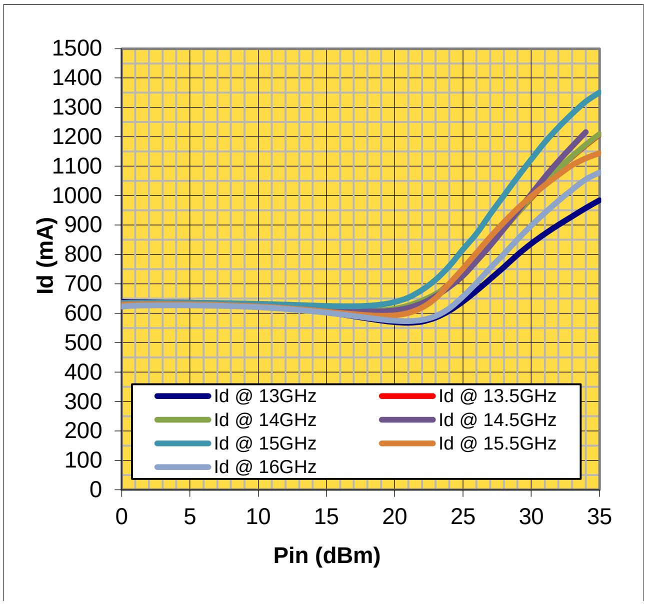
GAIN, Pout vs. Pin



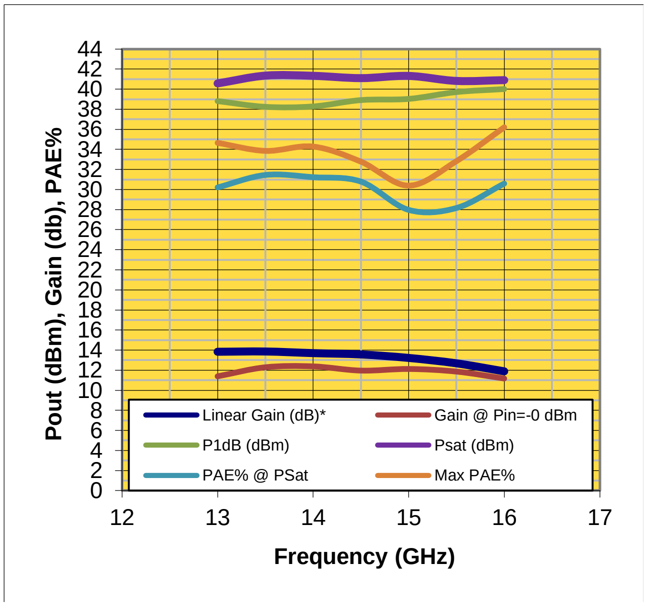
PAE vs. Pin



Id vs Pin



Pout, Gain, PAE vs. Frequency



**CW Fixture *On-wafer Pulsed Power

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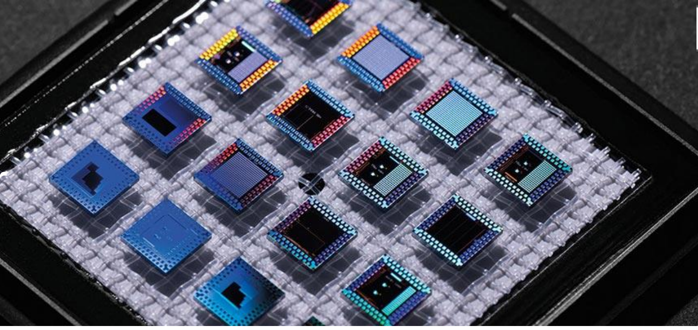

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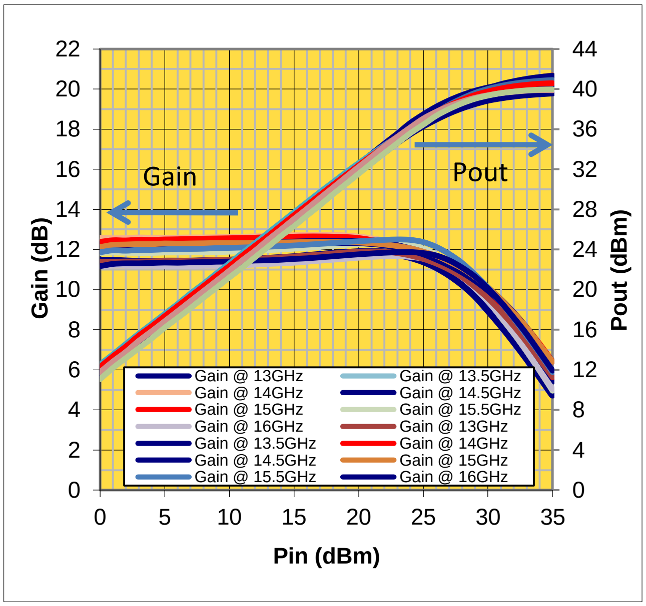
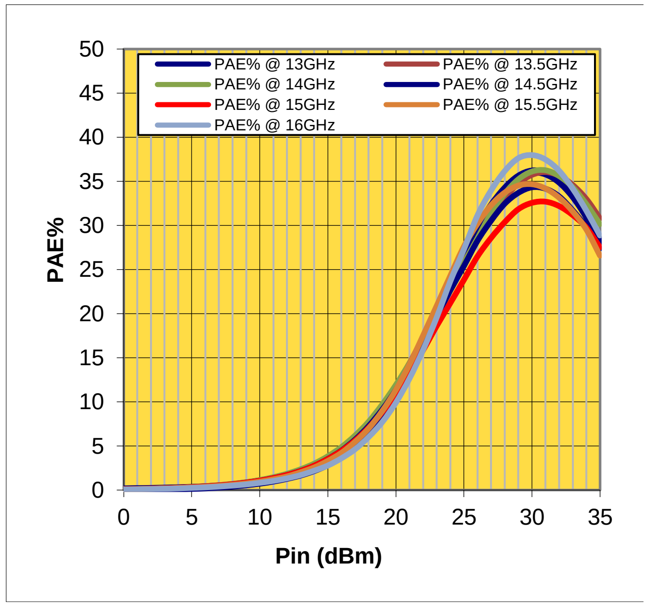
Measured fixture Performance Characteristics (Typical Performance at 25°C)
Vd = 24 V, Id = 640 mA. **

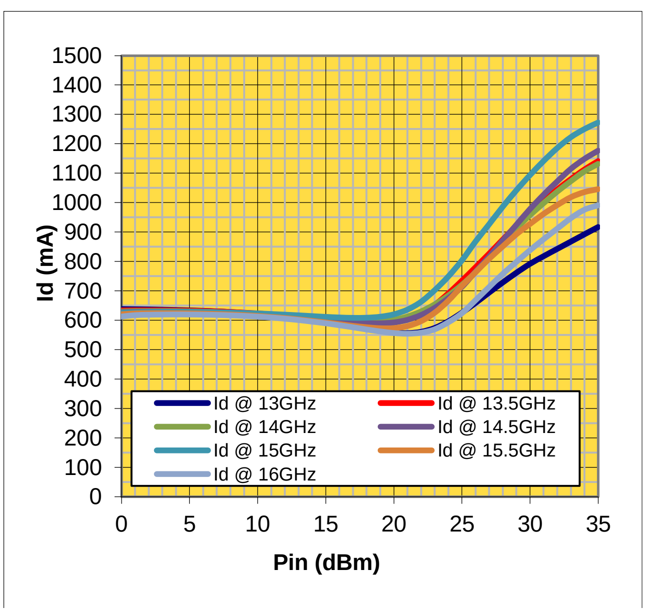
GAIN, Pout vs. Pin



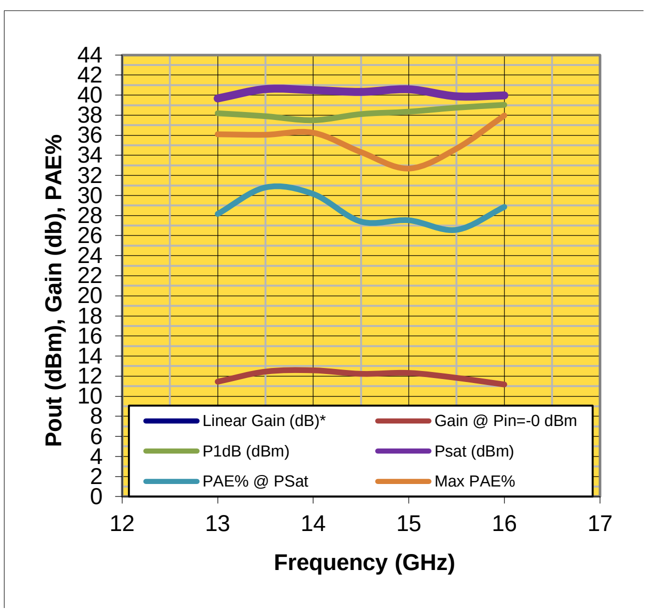
PAE vs. Pin



Id vs Pin



Pout, Gain, PAE vs. Frequency



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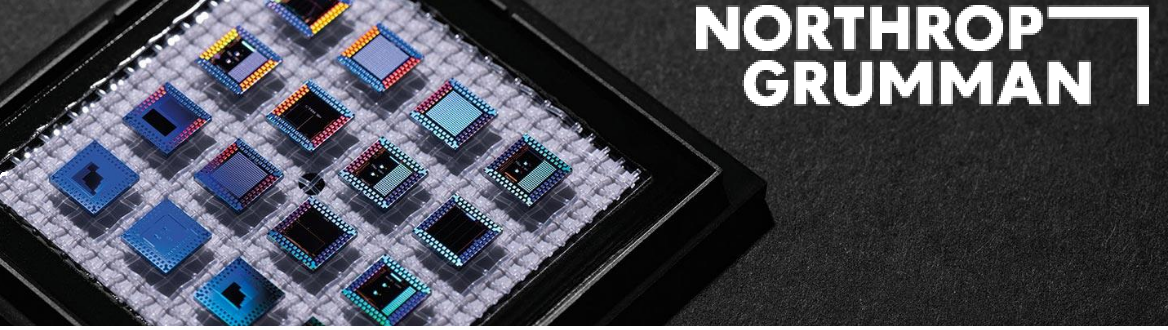

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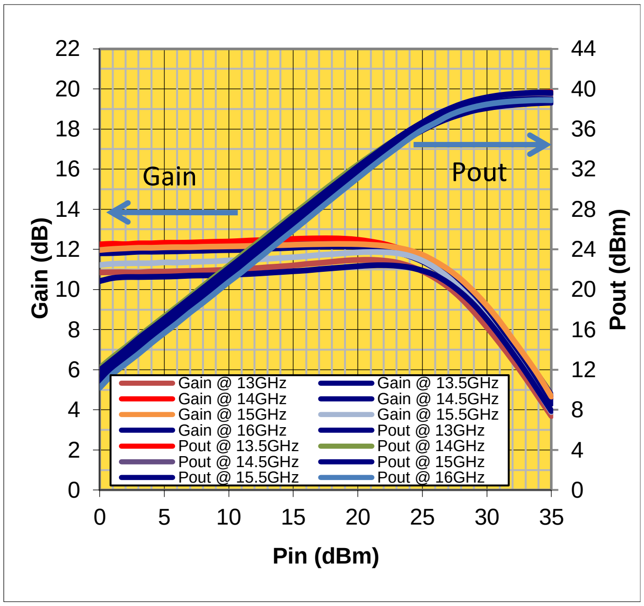
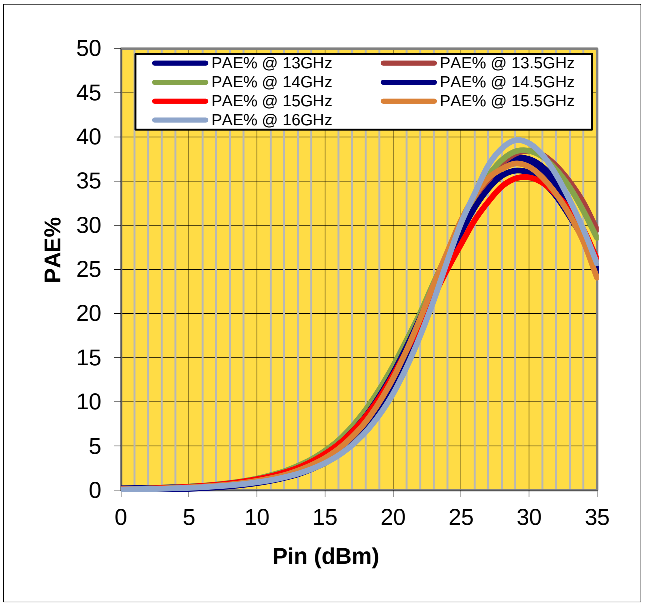
Measured fixture Performance Characteristics (Typical Performance at 25°C) Vd = 20 V, Id = 640 mA. **

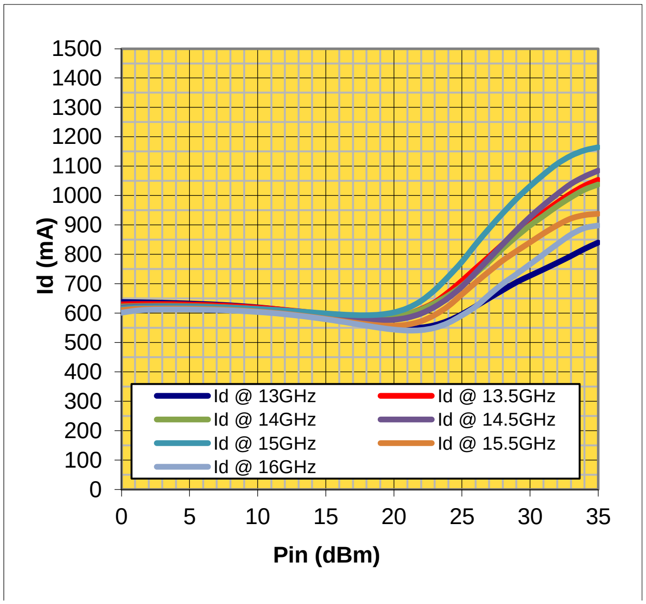
GAIN, Pout vs. Pin



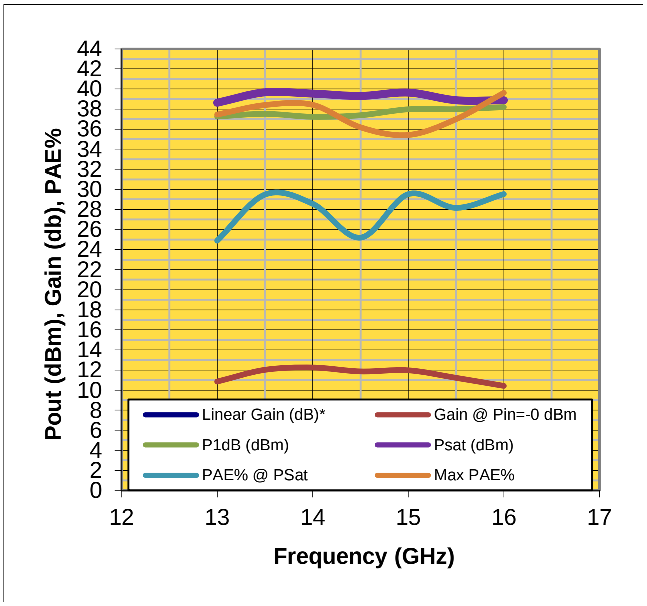
PAE vs. Pin



Id vs Pin



Pout, Gain, PAE vs. Frequency



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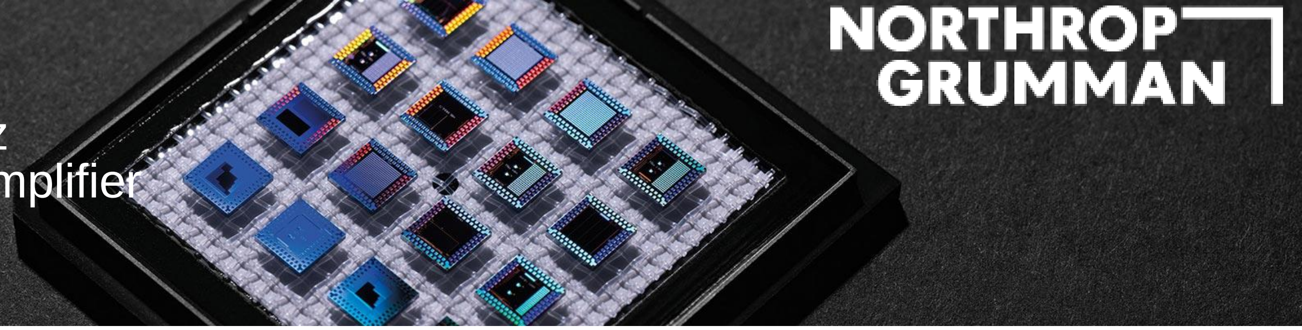
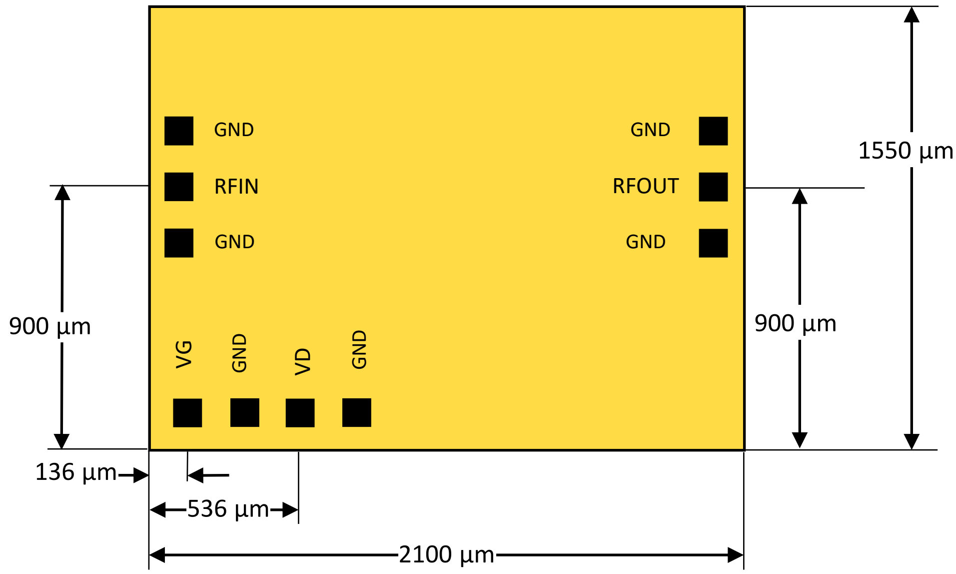


Die Size and Bond Pad Locations (Not to Scale)

X = 2100 ± 25 µm
Y = 1550 ± 25 µm
DC Bond Pad = 100 x 100 ± 0.5 µm
RF Bond Pad = 100 x 100 ± 0.5 µm
Chip Thickness = 101 ± 5 µm



Biasing/De-Biasing Details:
APN232 can only be biased at the bottom of the die.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
   i. Apply negative gate voltage (-5 V) to ensure that all devices are off
   ii. Ramp up drain bias to ~10 V
   iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
   iv. Ramp up drain to operating bias
   v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
   i. Gradually decrease drain bias to 0 V.
   ii. Gradually decrease gate bias to 0 V.
   iii. Turn off supply voltages

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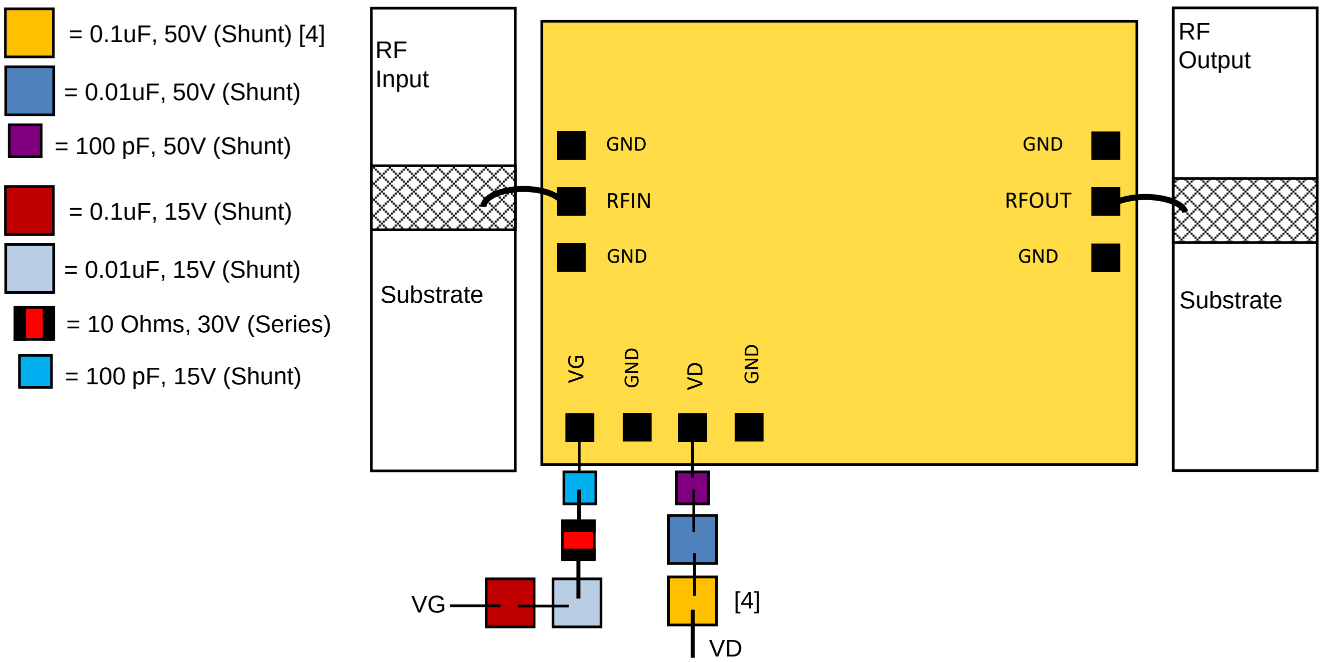
Suggested Bonding Arrangement



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most Northrop Grumman Aerospace Systems (NGAS) GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320ºC for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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