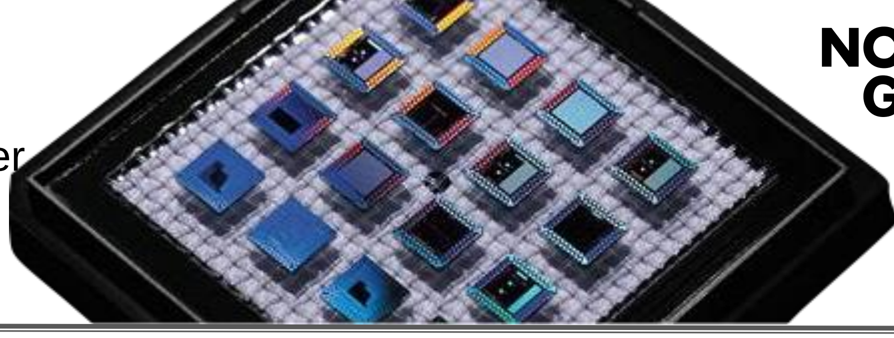
APN244

24 – 28 GHz
GaN Power Amplifier



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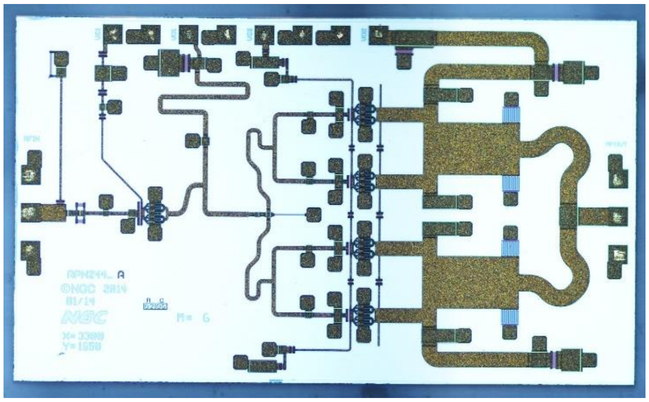

x=3.3 mm; y=1.95 mm

Product Description

The APN244 monolithic GaN HEMT amplifier is a broadband, two-stage power device, designed for use in Ka-Band communication applications such as point-to-point and point-to-multipoint digital (LMDS) radios and SatCom Terminals. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Applications

- Point-to-Point Digital Radios
- Point-to-Multipoint Digital Radios
- Space-Earth Communications
- Space Research & Earth Exploration

Product Features

- RF frequency: 24 to 28 GHz
- Linear Gain: 20 dB typ.
- Psat: ~7 W on wafer, typical
- Psat: ~7 W (CW @ 28V)
- Die Size: 6.43 sq. mm.
- 0.2um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 28 VDC @ 0.5 A

Export Information
ECCN: **3A001.b.2.c**
HTS (Schedule B) code: **8542.33.0001**

* Pulsed-Power On-Wafer unless otherwise noted

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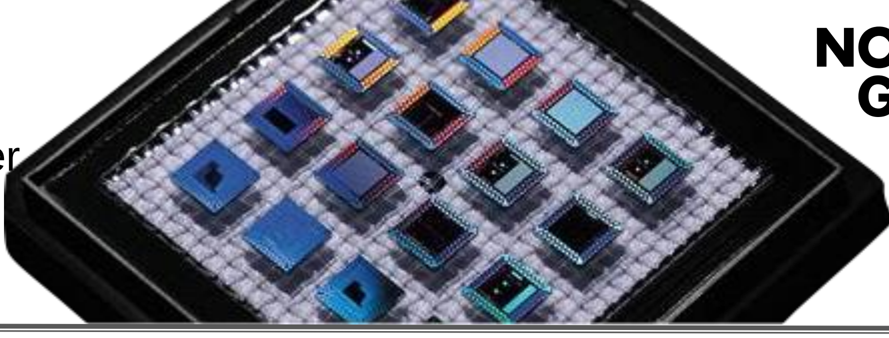

Absolute Maximum Ratings

Parameter	Value	Unit
Drain Voltage	28	V
Gate Voltage Range	-8 to 0	V
Drain Current	625	mA
Gate Current	0.25	mA
Power Dissipation*	17.5	W
Soldering Temperature	320	ºC

*7W/mm of gate periphery

Recommended Operating Conditions

Parameter	Value	Unit
Drain Voltage Range	20 - 28	V
Gate Voltage Range	-5 to -3	V
Stg 1 Drain Current (Idq)	100	mA
Stg 2 Drain Current (Idq)	100 - 400	mA

Electrical Specifications

Parameter	Min	Typ	Max	Unit
Operational Frequency	24		28	GHz
Small Signal at 28V				
Small Signal Linear Gain	18		21	dB
Input Return Loss	-21.8		-9	dB
Output Return Loss	-25		-5	dB
On-Wafer Pulsed Power at 28V				
Psat (at 27 dBm)	37.5	38.5	39.3	dBm
Power Gain (at 27 dBm)	10.5	11.5	12.4	dB
P1db	36	37	37.6	dBm
PAE (at 27 dBm)	23	25.3	28.3	%
Max PAE	26	27	28.3	%
Fixtured CW at 28V, 25ºC Case Temp				
Psat (at 26 dBm)	36.6	38.3	39.2	dBm
Power Gain (at 26 dBm)	12	17.2	19.4	dB
PAE (at 26 dBm)	19.3	24.5	35.2	%
Max PAE	23.5	30.3	35.2	%
Drain Voltage		28		V
Stage 1 Gate Voltage		-3.925		V
Stage 2 Gate Voltage		-3.950		V
Stage 1 Idq		100		mA
Stage 2 Idq		400		mA

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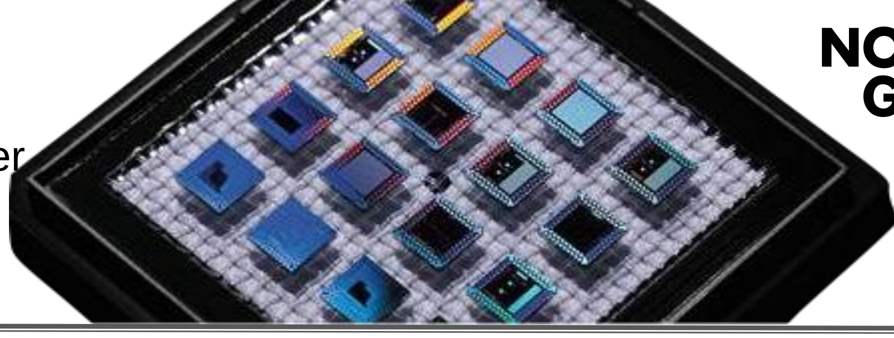

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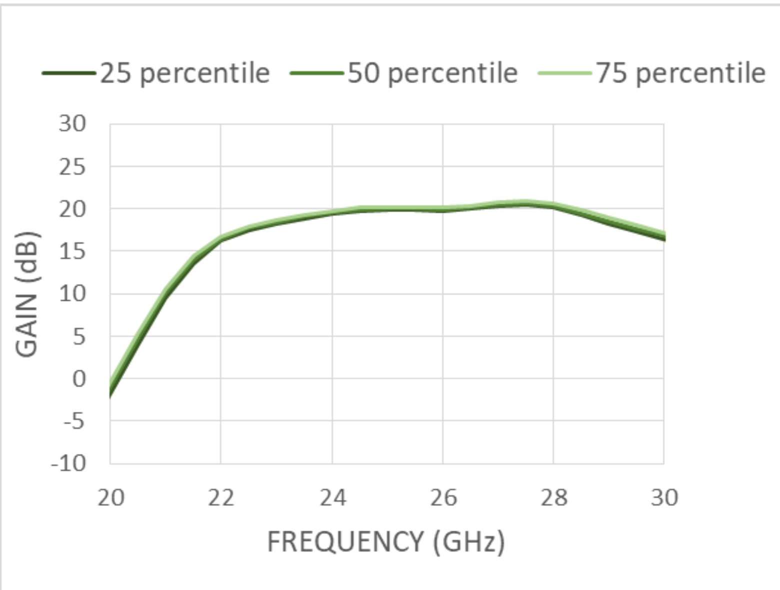
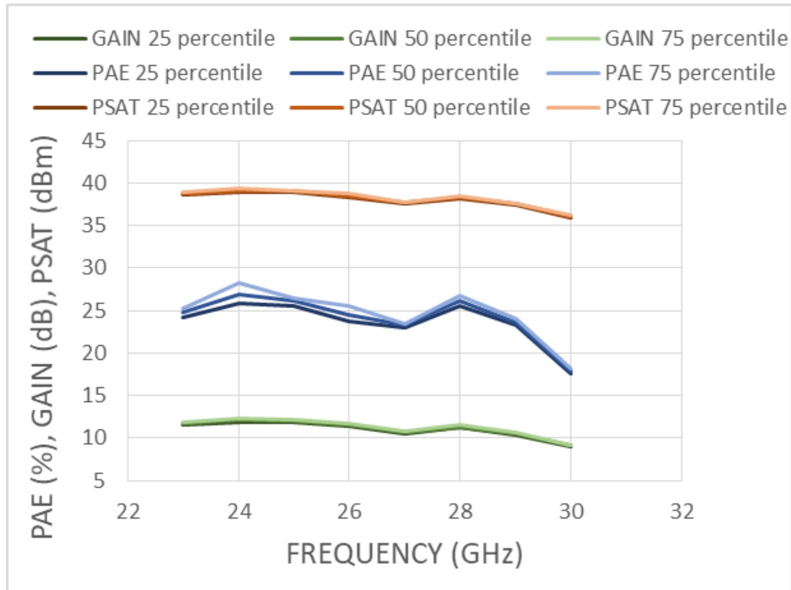
Pulsed on wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 100 mA, Id2 + Id2a = 400 mA

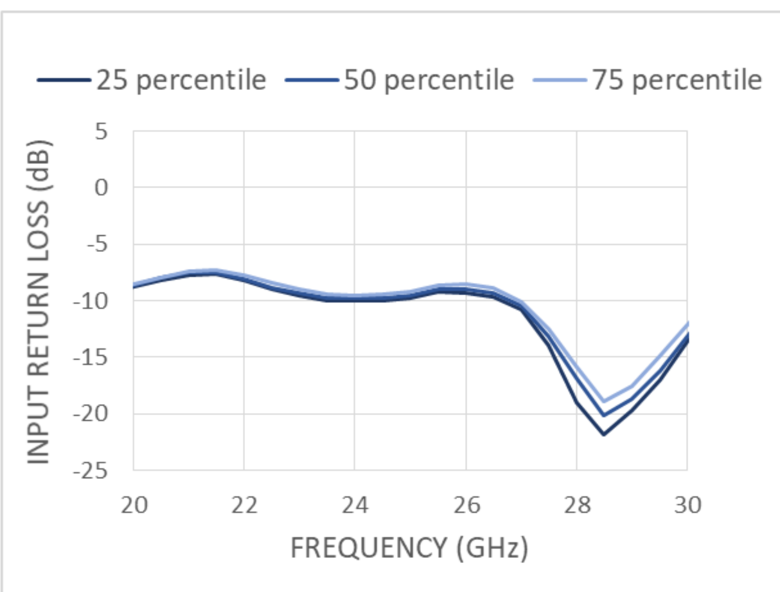
Small Signal GAIN vs. Frequency



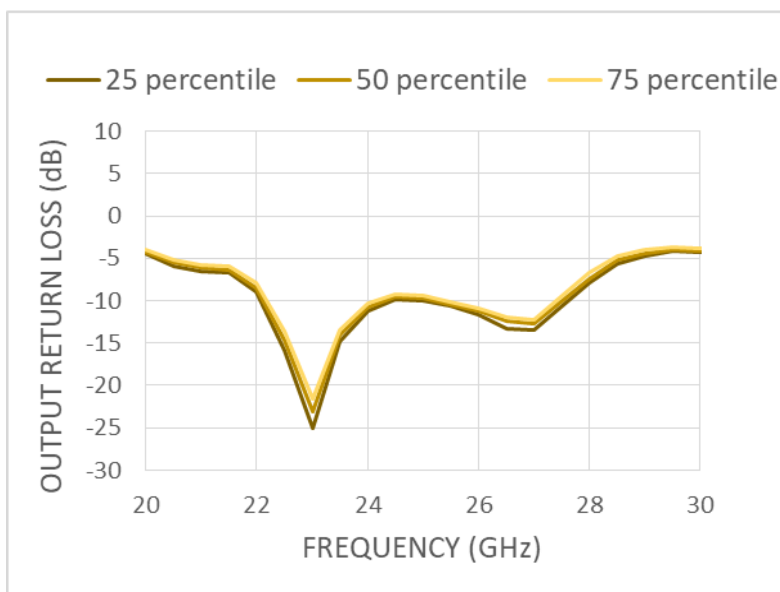
Large Signal PAE, GAIN, PSAT vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



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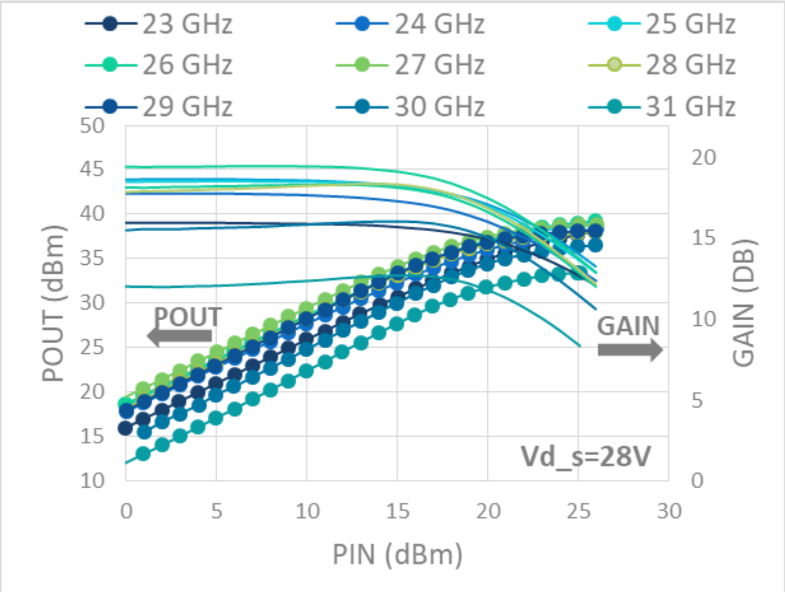
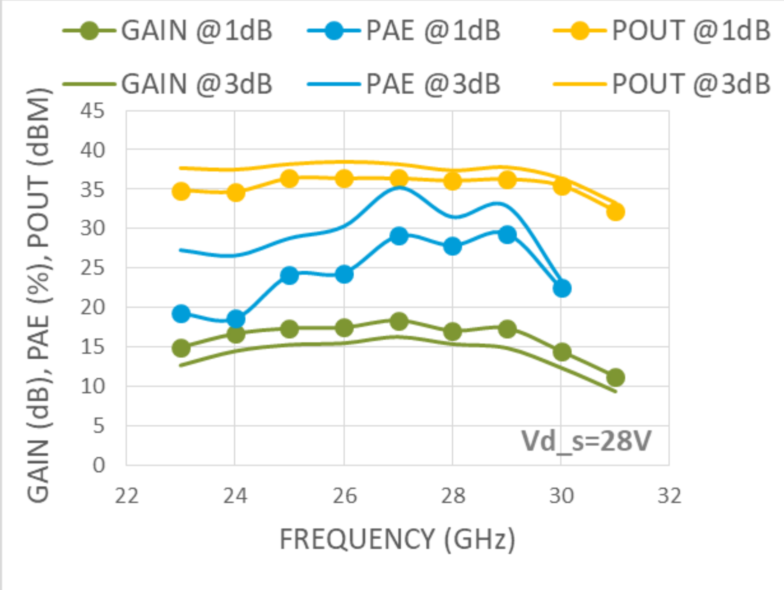
CW fixture measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 100mA, Id2 + Id2a =400 mA

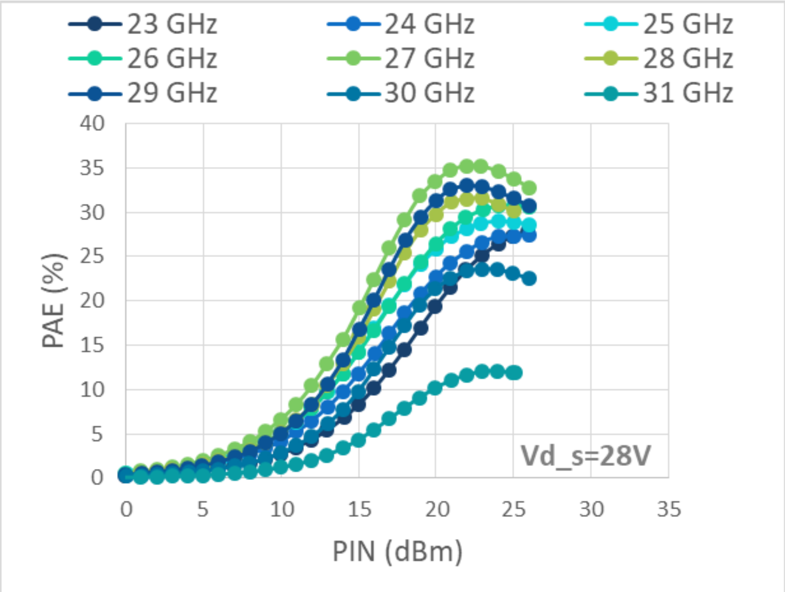
POUT and GAIN vs. PIN



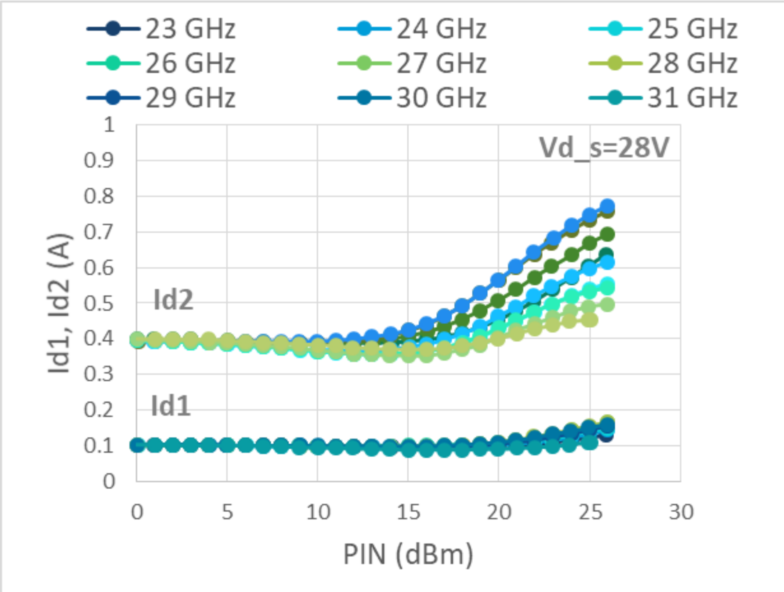
PAE, GAIN, POUT vs. FREQUENCY



PAE vs PIN



Id1, Id2 vs PIN



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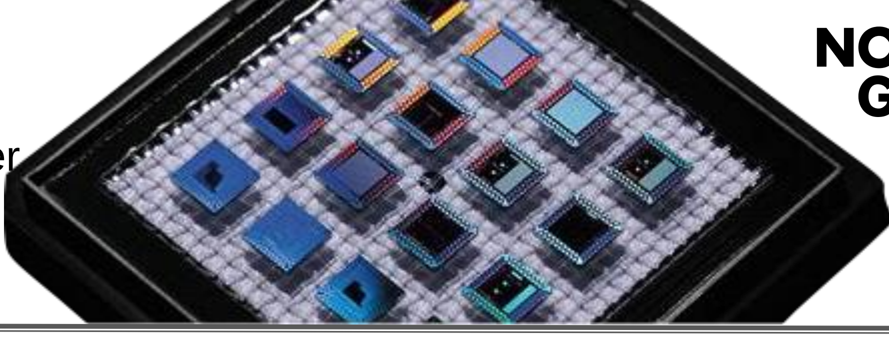

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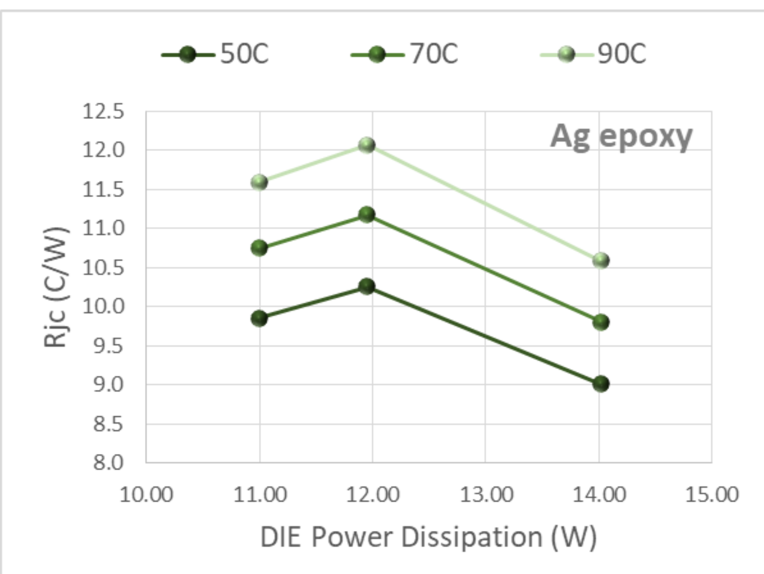
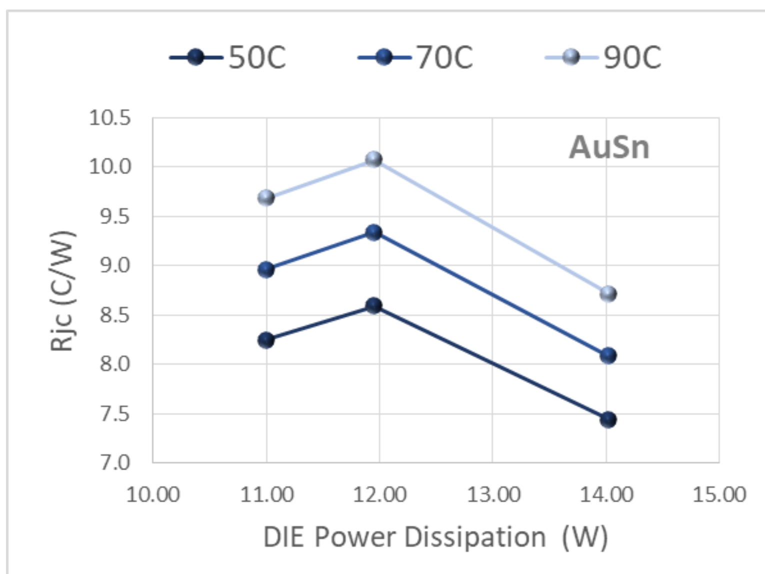
Preliminary Thermal Properties with die mounted with 25um 80/20 AuSn Eutectic to: 10mil Cu10W Shim.

Shim	Mounting Material	Average Backside Die Temperature	Hottest Junction Temperature Tjc	RF Output	Power Dissipation (W)	Thermal Resistance Rjc (ºC/W)
10 mil CuW	AuSn Eutectic	50 ºC	154.3	39.7	11.0	7.4
			152.7	36.7	12.0	8.6
			140.7	33.7	14.0	8.2
		70 ºC	183.3	39.7	11.0	8.1
			181.7	36.7	12.0	9.3
			168.5	33.7	14.0	9.0
		90 ºC	212.2	39.7	11.0	8.7
			210.5	36.7	12.0	10.1
			196.5	33.7	14.0	9.7
10 mil CuW	Ag Epoxy	50 ºC	158.3	39.7	11.0	9.9
			172.6	36.7	12.0	10.3
			176.3	33.7	14.0	9.0
		70 ºC	188.1	39.7	11.0	10.7
			203.5	36.7	12.0	11.2
			207.5	33.7	14.0	9.8
		90 ºC	217.5	33.71	11.0	11.6
			234.2	36.73	12.0	12.1
			238.4	39.70	14.0	10.6





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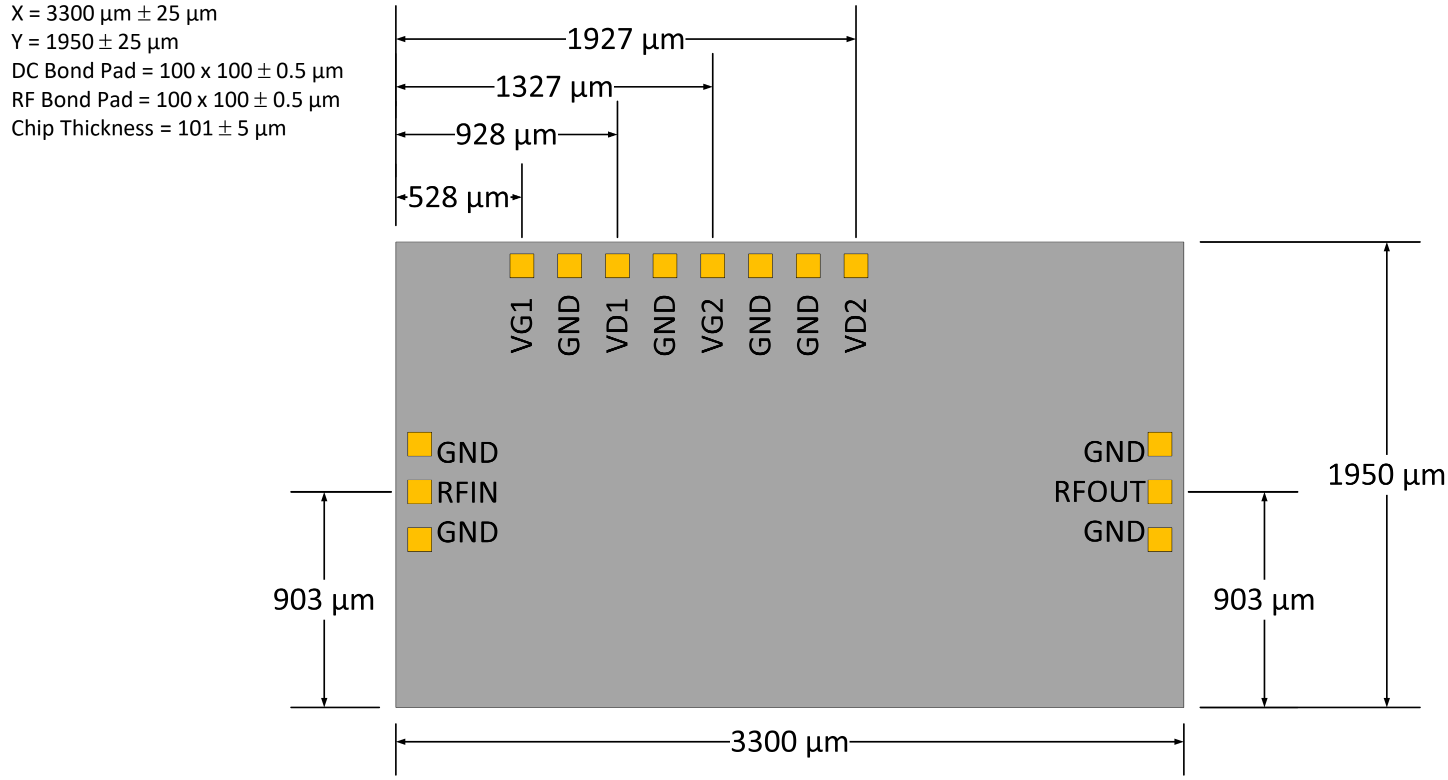
Die Size and Bond Pad Locations (Not to Scale)



Biasing/De-Biasing Details:

Bias is single sided and is from the top only.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-8 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
    i. Gradually decrease drain bias to 0 V.
    ii. Gradually decrease gate bias to 0 V.
    iii. Turn off supply voltages
f. Repeat de-bias procedure for each amplifier stage

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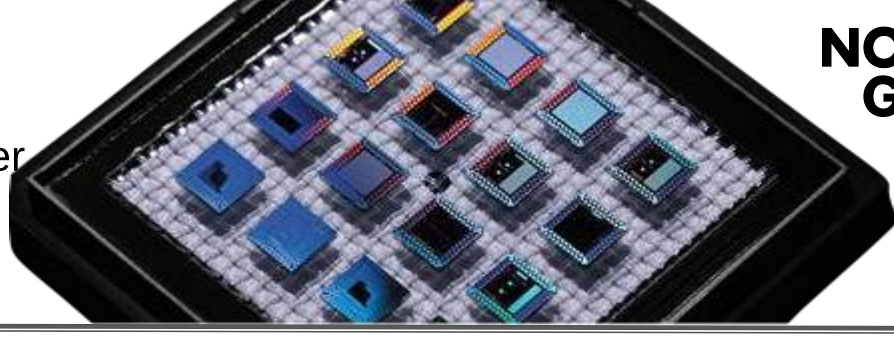

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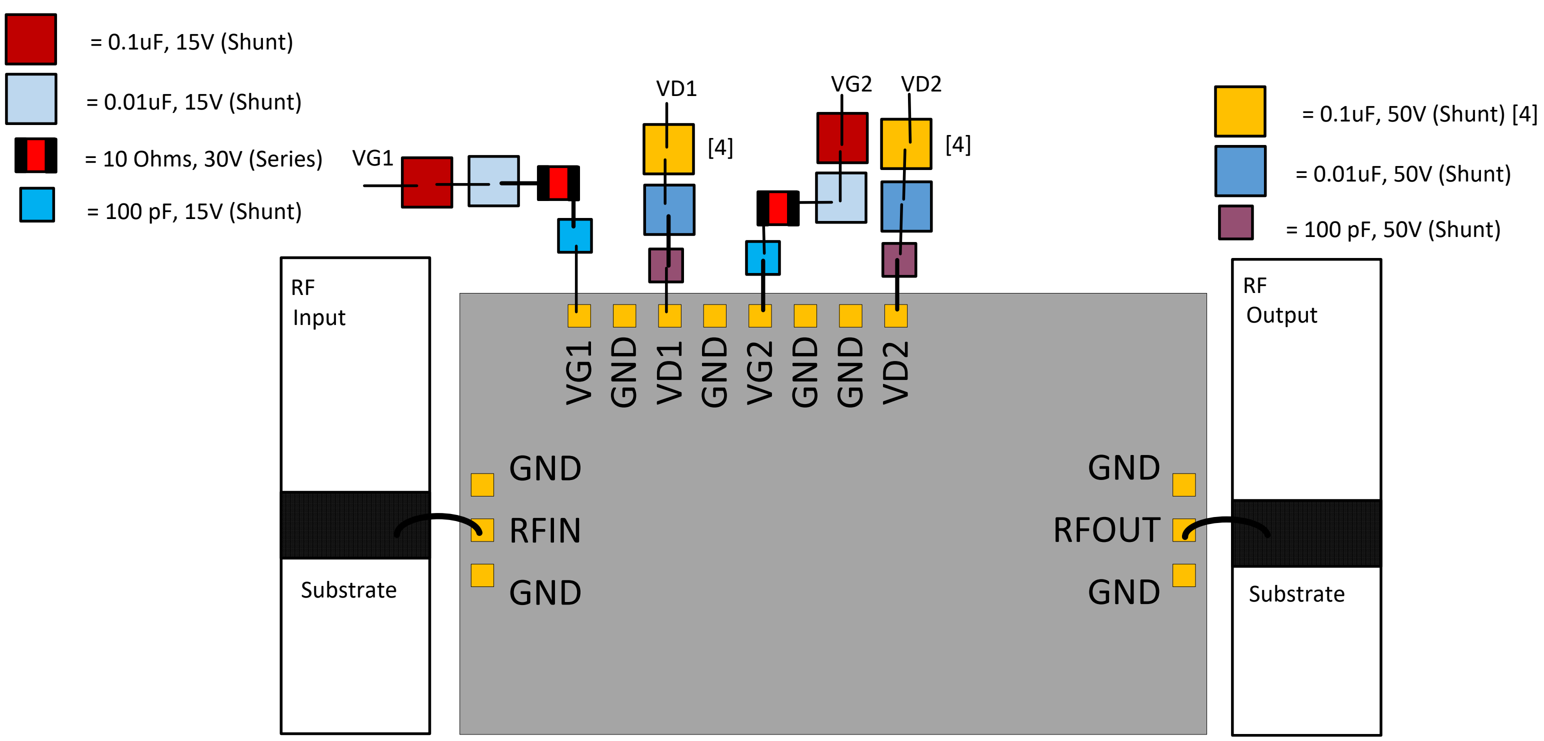
Suggested Bonding Arrangement



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most NGAS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320ºC for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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