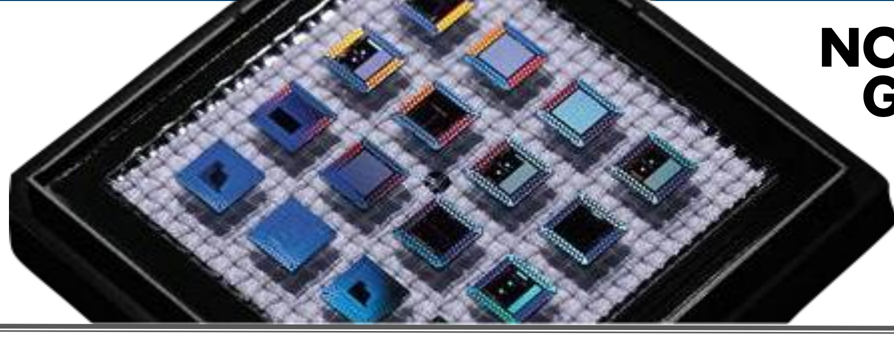
APN252
10–14 GHz
GaN Driver Amplifier



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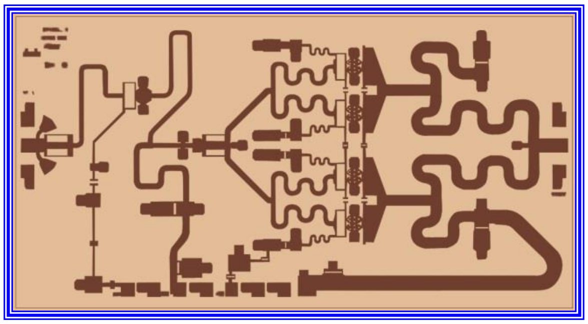

X = 4.3 mm Y = 2.3 mm

Product Description

The APN252 monolithic GaN HEMT amplifier is a broadband, 2 Stage power device, designed for use in SATCOM Terminals and point-to-point digital radios. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Applications

- Electronic Warfare
- Radar
- Test Equipment

Product Features

- RF frequency: 10 to 14 GHz
- Linear Gain: 25.5 typ.*
- P1dB: 34 dBm typ.*
- Psat: 38 dBm typ.*
- PAE% @ Psat: 40% typ.*
- Die Size: 9.46 sq. mm
- 0.2 um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 24 VDC @ 480 mA

Export Information
ECCN: **3A001.b.2.b.2**
HTS (Schedule B) code: **8542.33.0000**

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Absolute Maximum Ratings

Parameter	Value	Unit
Drain Voltage	28	V
Gate Voltage Range	-8 to 0	V
Drain Current	600	mA
Gate Current	0.24	mA
Soldering Temperature	320	ºC

Recommended Operating Conditions

Parameter	Value	Unit
Drain Voltage Range	20 - 28	V
Gate Voltage Range	-5 to -3	V
Stg 1 Drain Current (Idq)	80	mA
Stg 2 Drain Current (Idq)	100 - 400	mA

Electrical Specifications

Parameter	Min	Typ	Max	Unit
Operational Frequency	10		14	GHz
Small Signal at 22V				
Small Signal Linear Gain	24	25	26	dB
Input Return Loss	-23		-10	dB
Output Return Loss	-9		-2	dB
On-Wafer Pulsed Power at 22V				
Psat (at 20 dBm)	37.3		38.4	dBm
Power Gain (at 20 dBm)	17.3	18	18.4	dB
P1db	34		36	dBm
PAE (at 20 dBm)	32.4		40.6	%
Max PAE	33.5		40.6	%
Fixtured CW at 22V, 25ºC Case Temp				
Psat (at 20 dBm)	36.8		37.5	dBm
Power Gain (at 20 dBm)	25.4		26	dB
PAE (at 20 dBm)	32		38	%
Max PAE			38.6	%
Drain Voltage		22		V
Stage 1 Gate Voltage		-3.785		V
Stage 2 Gate Voltage		-3.745		V
Stage 1 Idq		80		mA
Stage 2 Idq		400		mA

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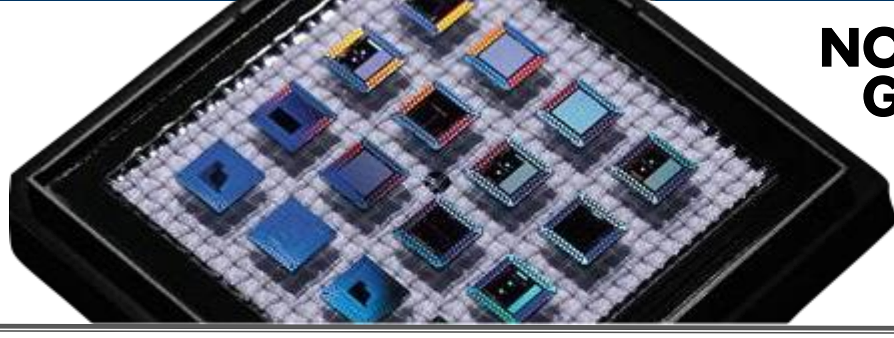
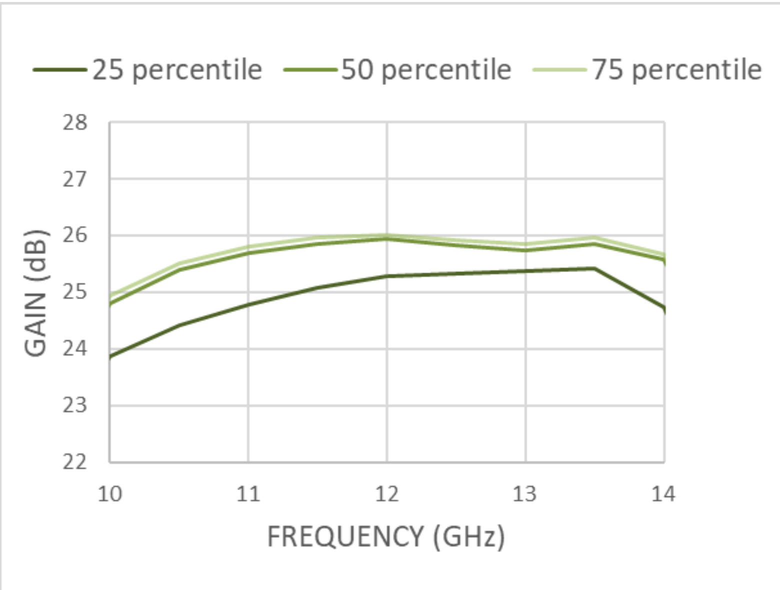
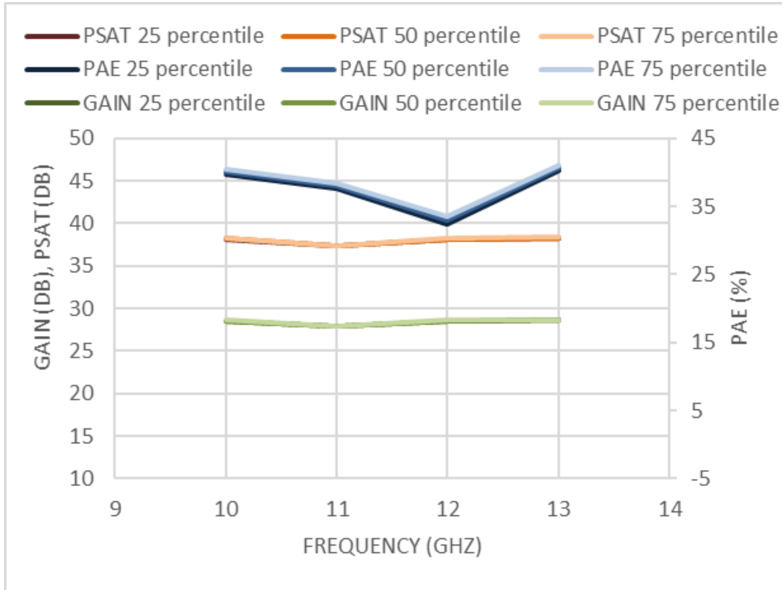


On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd1 = Vd2 = 22 V, Id1 = 80 mA, Id2 = 400 mA

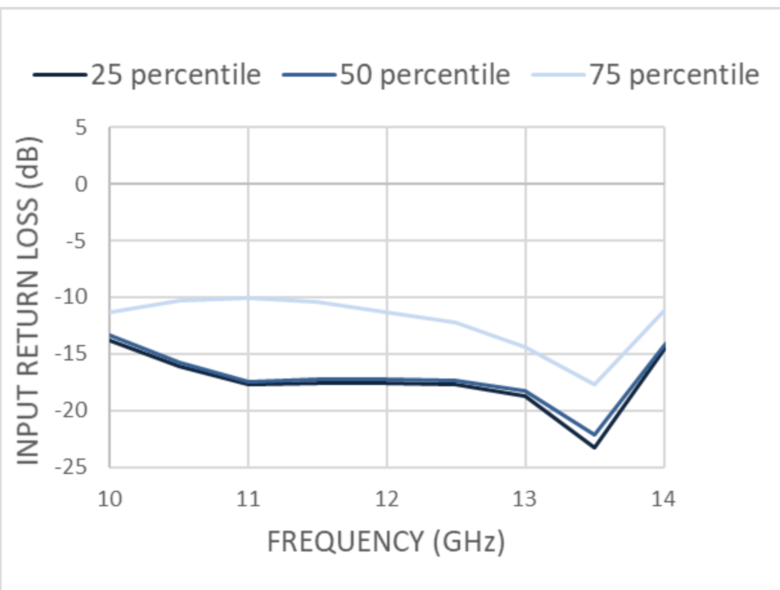
GAIN vs. Frequency



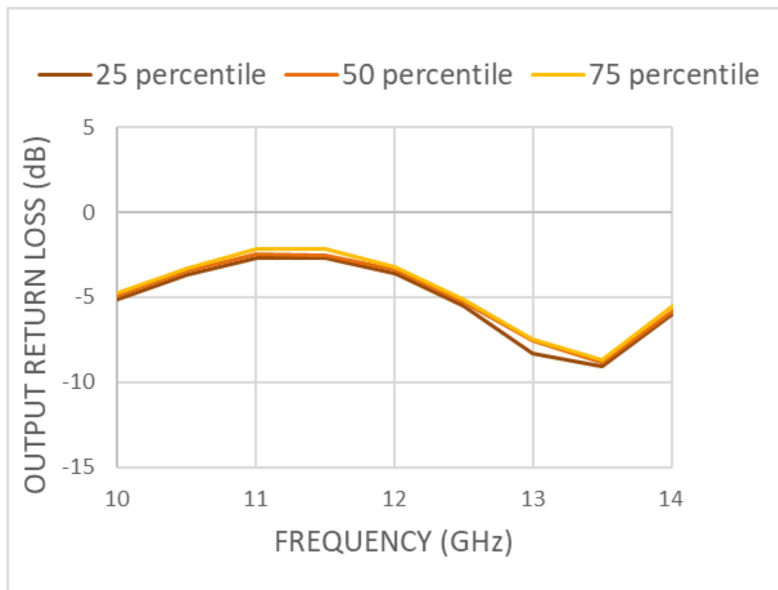
PAE, GAIN, Pout vs. Frequency **



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



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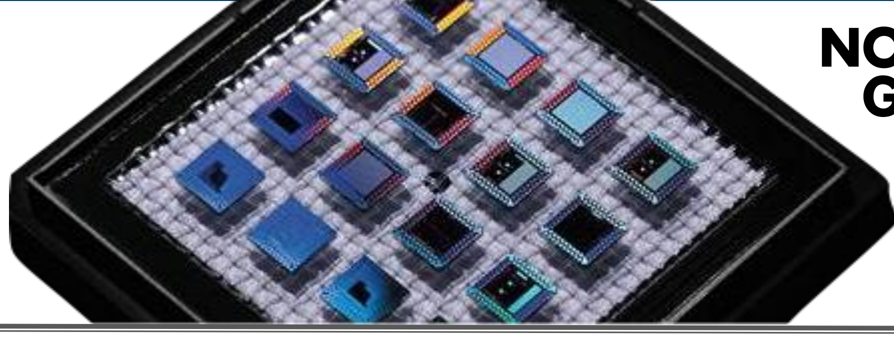
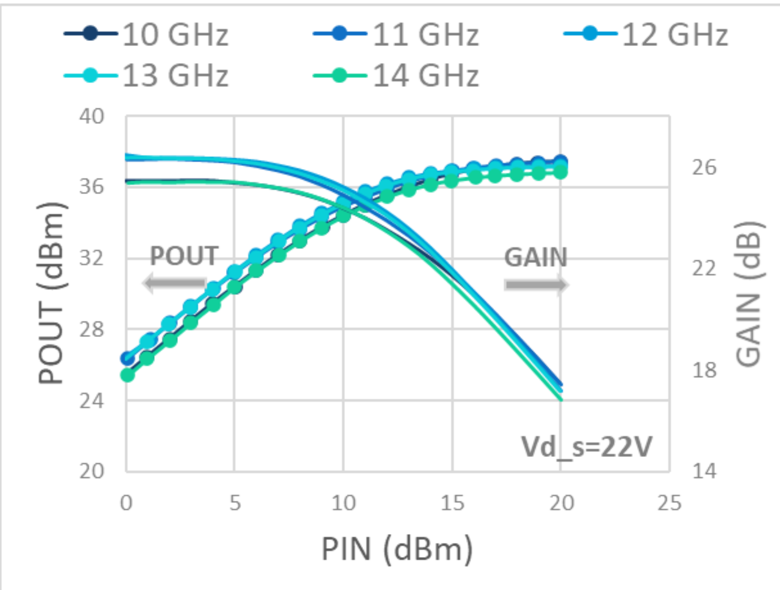
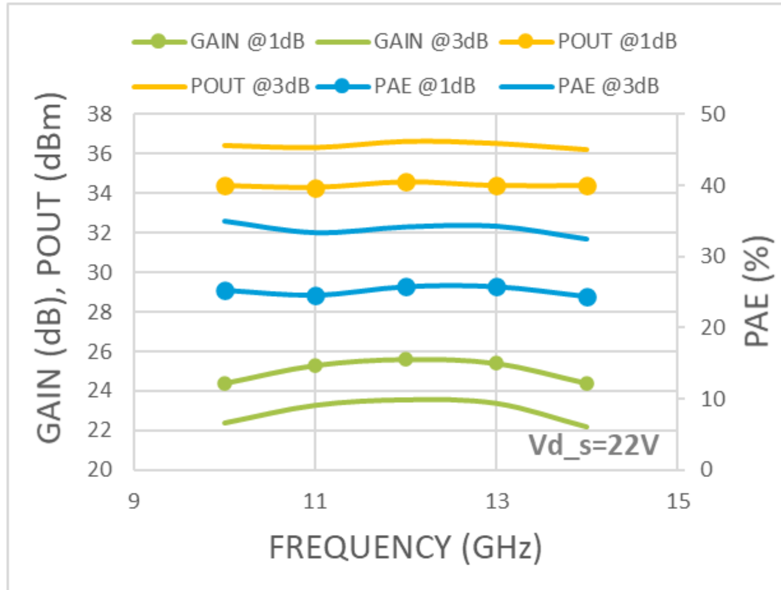


Fixture measured Performance Characteristics (Typical Performance at 25°C)
Vd = 22 V, Id1 = 80 mA, Id2 = 400 mA

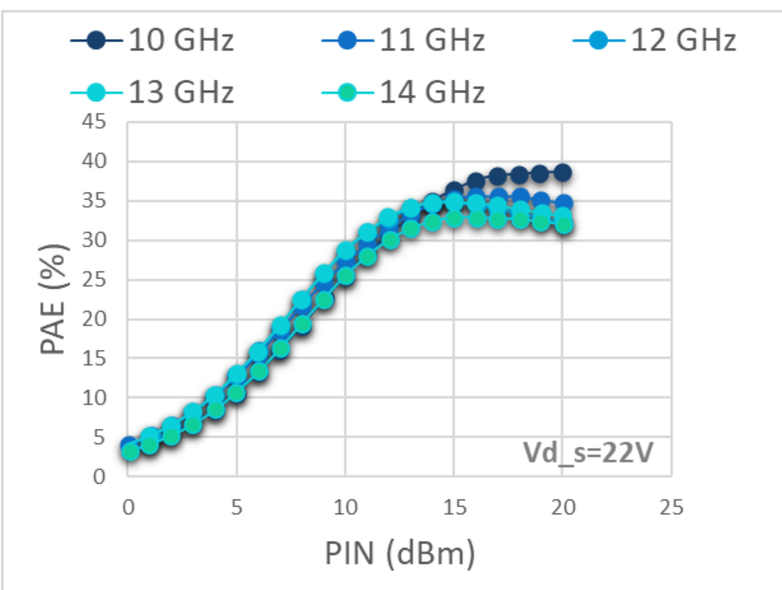
POUT and GAIN vs. PIN



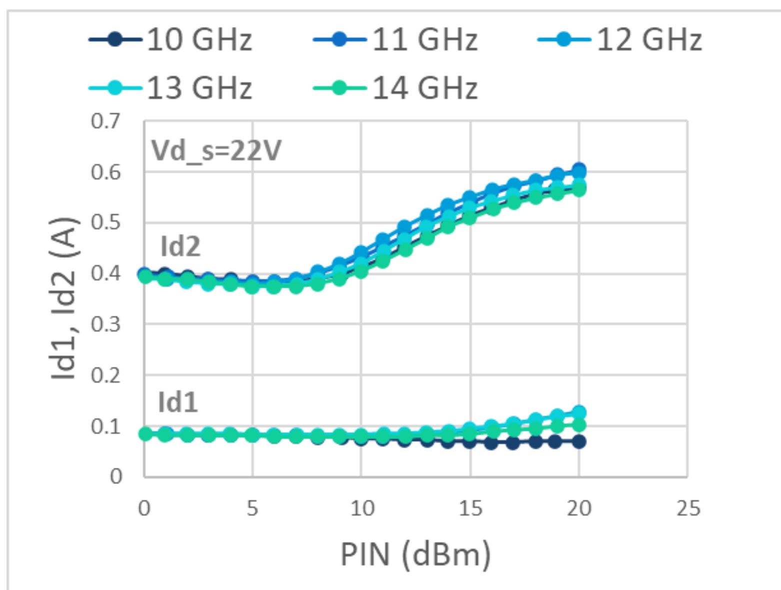
PAE, GAIN, POUT vs. FREQUENCY

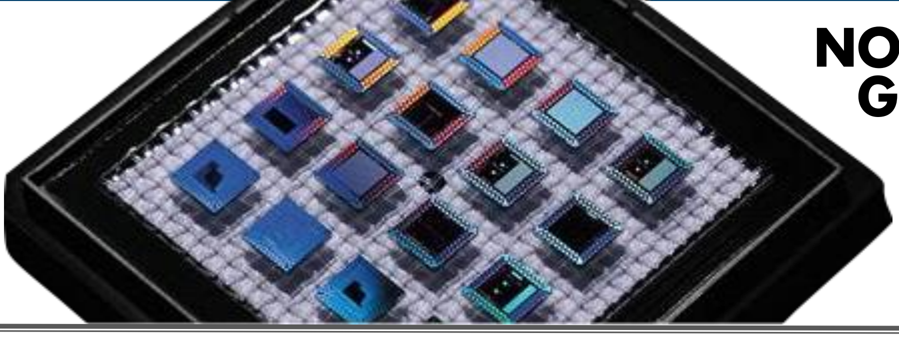


PAE vs PIN



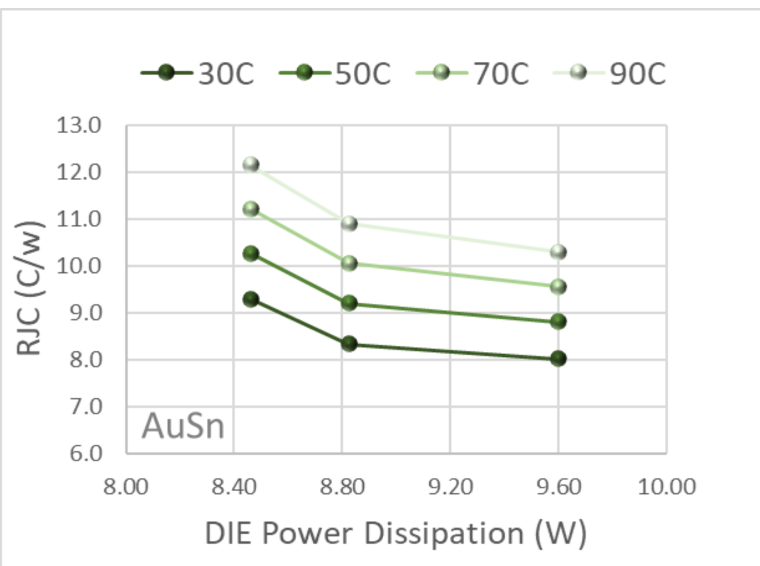
Id1, Id2 vs PIN

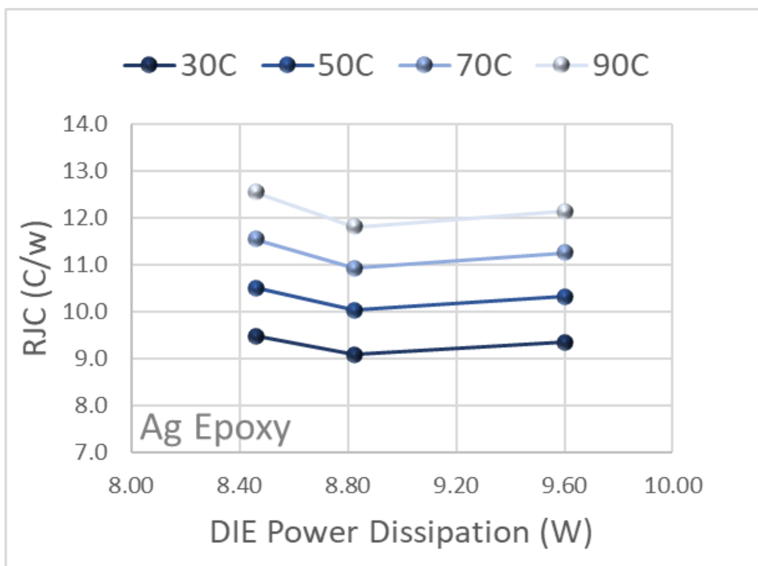


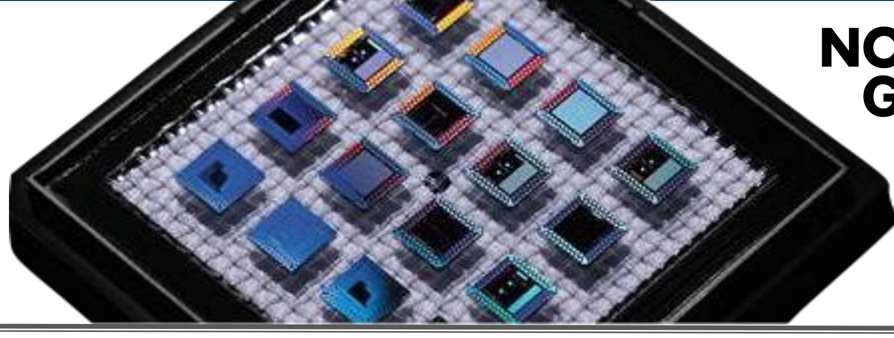


Preliminary Thermal Properties with die mounted with 25um 80/20 AuSn Eutectic to: 10mil Cu10W Shim.

Shim	Mounting Material	Average Backside Die Temperature	Hottest Junction Temperature Tjc	RF Output	Power Dissipation (W)	Thermal Resistance Rjc (ºC/W)
10 mil CuW	AuSn Eutectic	30 ºC	109	34.9	8.5	9.3
			103	36.6	8.8	8.3
			107	37.3	9.6	8.0
		50 ºC	137	34.9	8.5	10.3
			131	36.6	8.8	9.2
			134	37.3	9.6	8.8
		70 ºC	165	34.9	8.5	11.2
			159	36.6	8.8	10.0
			162	37.3	9.6	9.5
		90 ºC	193	34.9	8.5	12.1
			186	36.6	8.8	10.9
			189	37.3	9.6	10.3
10 mil CuW	Ag Epoxy	30 ºC	110	34.9	8.5	9.5
			110	36.6	8.8	9.1
			120	37.3	9.6	9.4
		50 ºC	139	34.9	8.5	10.5
			138	36.6	8.8	10.0
			149	37.3	9.6	10.3
		70 ºC	168	34.9	8.5	11.5
			166	36.6	8.8	10.9
			178	37.3	9.6	11.3
		90 ºC	196	34.9	8.5	12.5
			194	36.6	8.8	11.8
			207	37.3	9.6	12.8







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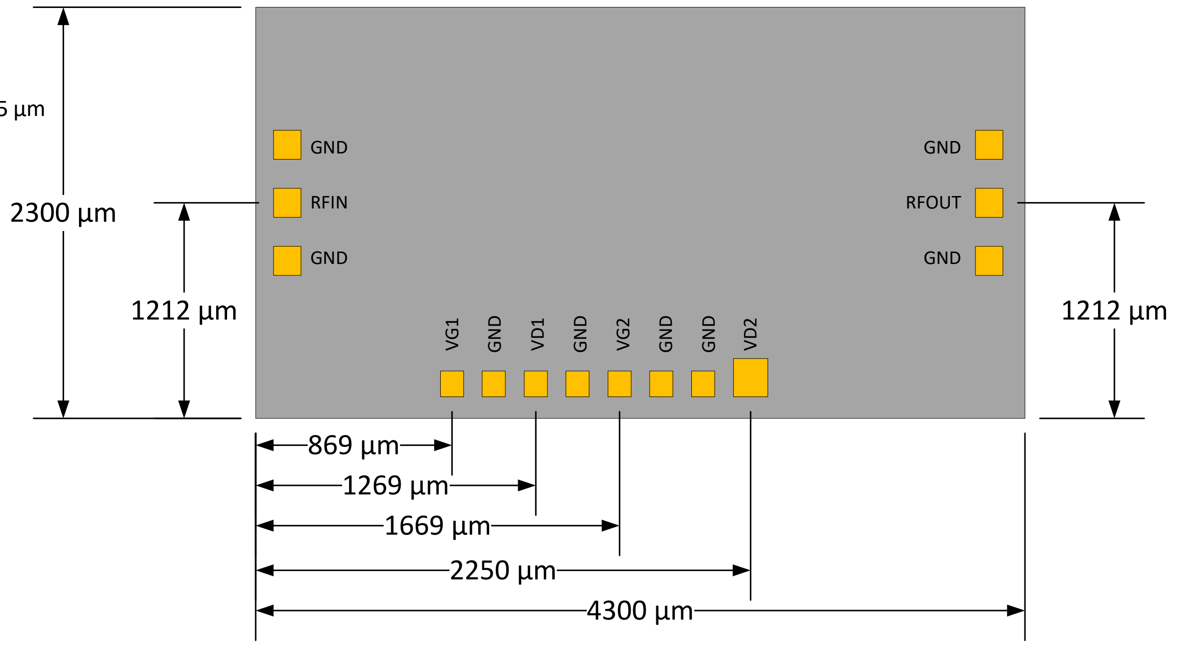
Die Size and Bond Pad Locations (Not to Scale)

X = 4300 ± 25 µm
Y = 2300 ± 25 µm
DC Bond Pad = 100 x 100 ± 0.5 µm
VD2 DC Bond Pad = 140 x 140 ± 0.5 µm
RF Bond Pad = 100 x 100 ± 0.5 µm
Chip Thickness = 101 ± 5 µm



Biasing/De-Biasing Details:
APN252 can be biased only from the bottom of the die.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-8 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. Repeat bias procedure for each amplifier stage
f. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
    i. Gradually decrease drain bias to 0 V.
    ii. Gradually decrease gate bias to 0 V.
    iii. Turn off supply voltages
g. Repeat de-bias procedure for each amplifier stage

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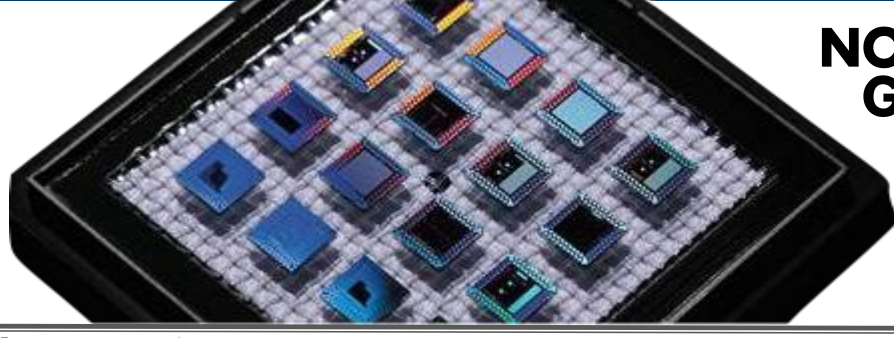
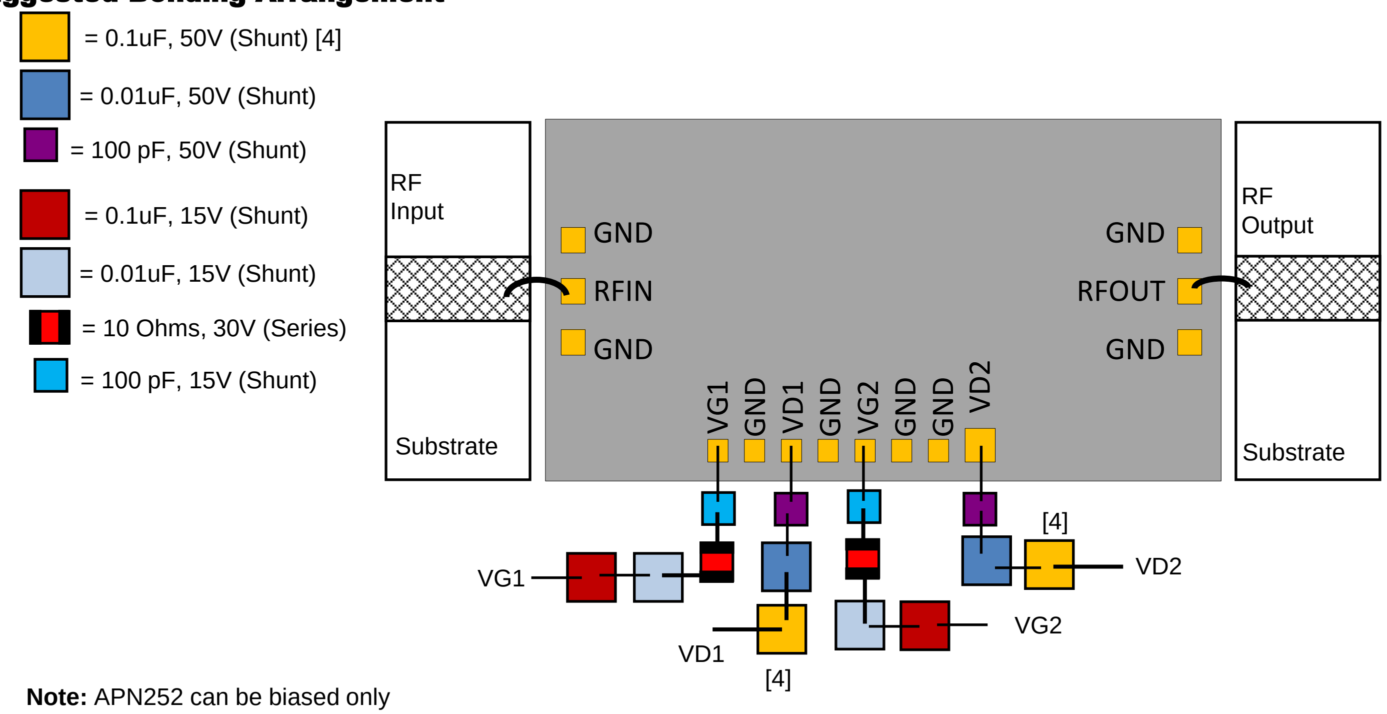


Suggested Bonding Arrangement



Note: APN252 can be biased only from the bottom of the die.

Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides if indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most Northrop Grumman Aerospace Systems (NGAS) GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320^{o}C for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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