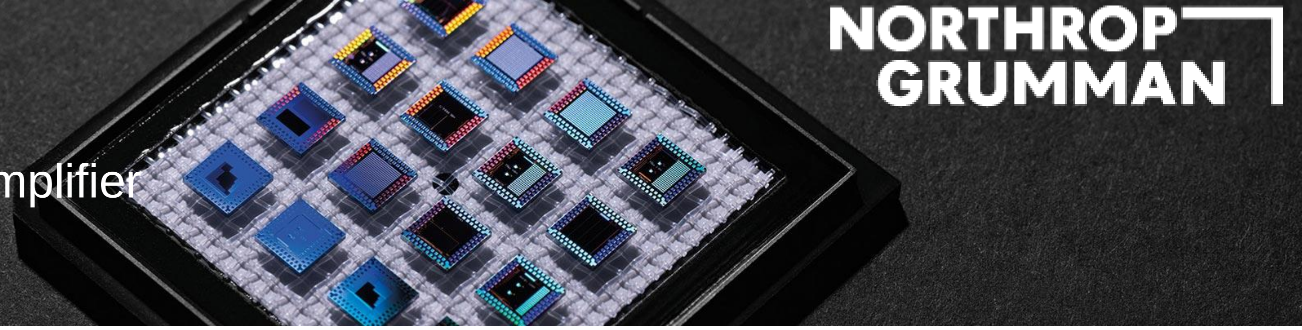

# APN267
## 2-18 GHz
## GaN Power Amplifier

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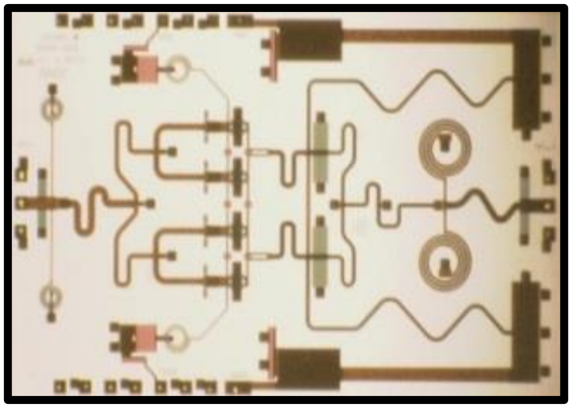

**X = 4.4 mm Y = 2.8 mm**

## Applications

- Electronic Warfare
- Radar
- Test Equipment

## Product Description

The APN267 distributed GaN HEMT amplifier is a broadband, one-stage power device, designed for use in electronic warfare and test equipments. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

## Product Features

- RF frequency:  2 to 18 GHz
- Linear Gain: 10-13 dB across the band
- Psat: 38-40 dBm across the band
- Die Size: 12.32 sq. mm
- 0.2 um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 24 VDC @ 480 mA

**Performance Characteristics (Ta = 25°C)**

| Specification * | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Frequency | 2 | | 18 | GHz |
| Linear Gain | 10 | 11 | 13 | dB |
| Input Return Loss | 2 | 8 | 12 | dB |
| Output Return Loss | 4 | 14 | 26 | dB |
| P1dB (PP*) | | 35 | | dBm |
| Psat (PP*) | 38 | 38.2 | 40 | dBm |
| PAE @Psat (PP*) | 25 | 33 | 38 | % |
| P1dB (CW) | | 36.2 | | dBm |
| Psat (CW) | 35 | 38.2 | 40 | dBm |
| PAE @Psat (CW) | | 25.5 | | % |
| Vd1=Vd1a | | 24 | | V |
| Vg1. Vg1a | | -3.5 | | V |
| Id1+Id1a | | 480 | | mA |





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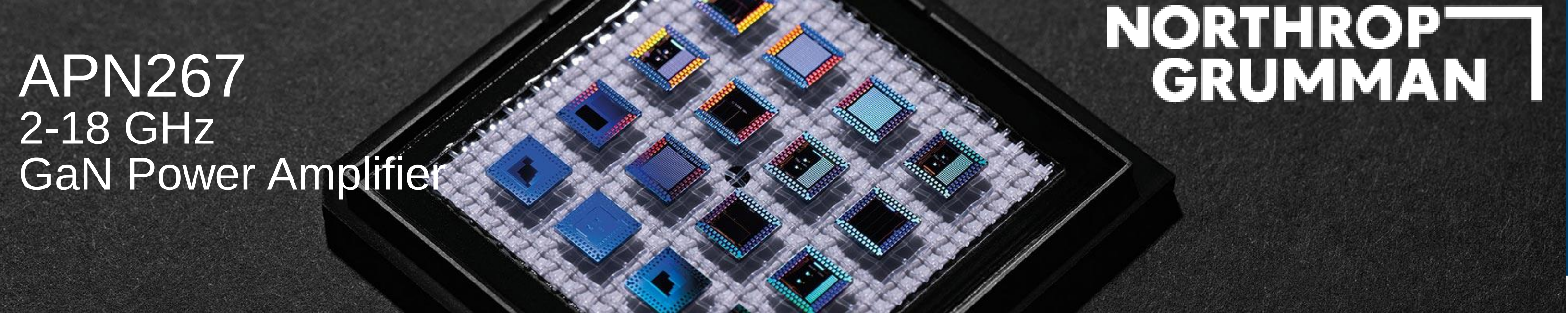

# APN267
## 2-18 GHz
## GaN Power Amplifier

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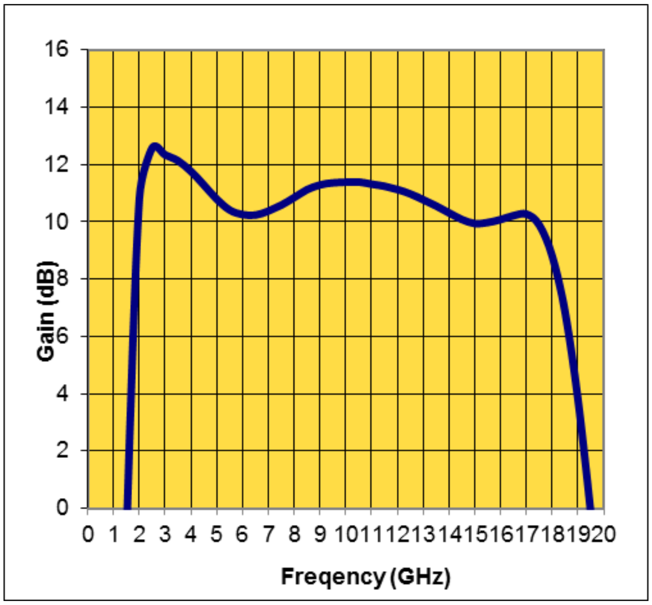
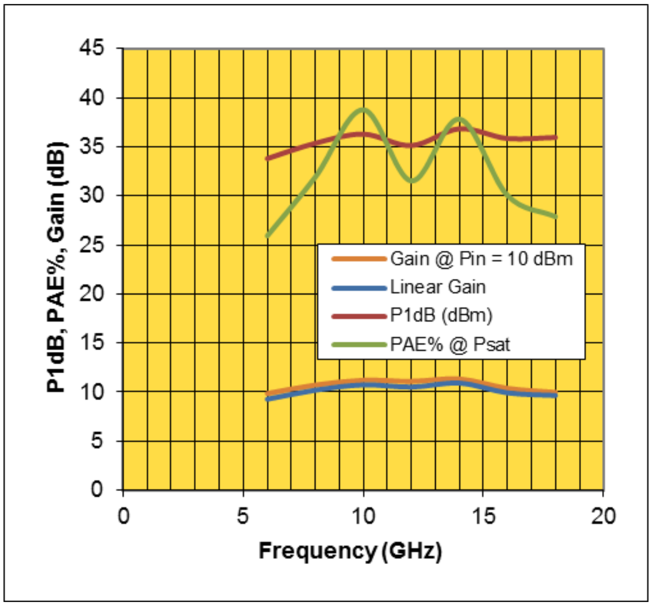
**On wafer measured Performance Characteristics (Typical Performance at 25°C)**
**Vd = 24.0 V, Id1 + Id1a = 480 mA.**

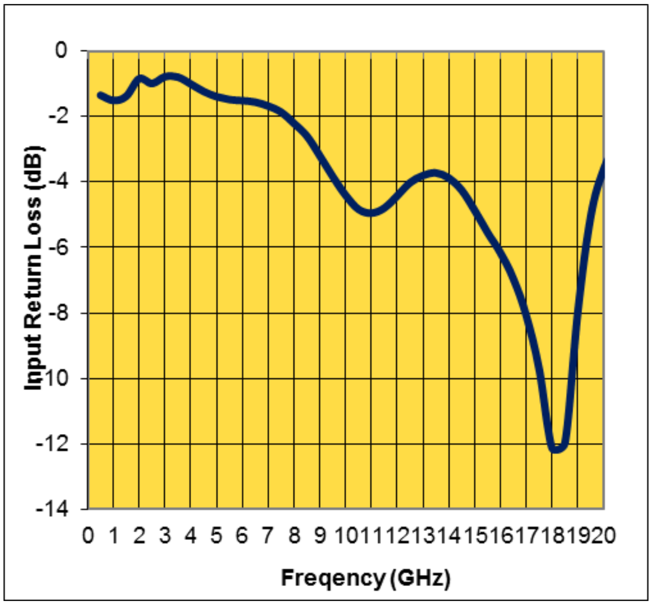
GAIN vs. Frequency



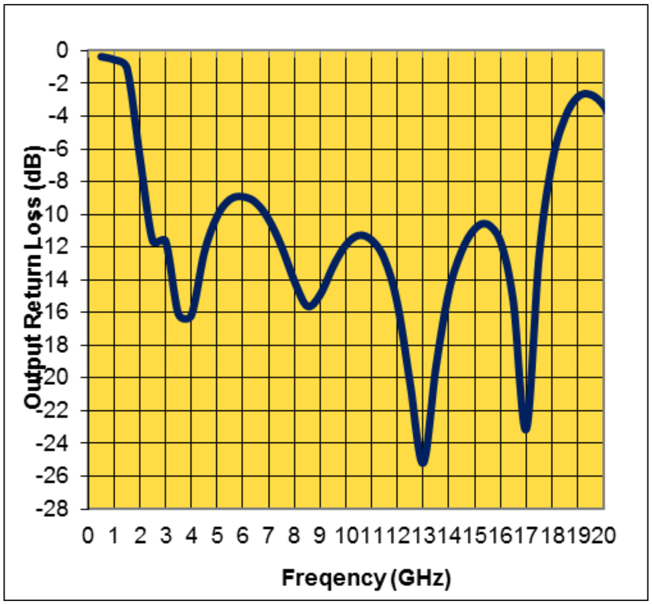

PAE, GAIN, P1dB vs. Frequency **




Input Return Loss vs. Frequency




Output Return Loss vs. Frequency




*Pulsed-power on-wafer

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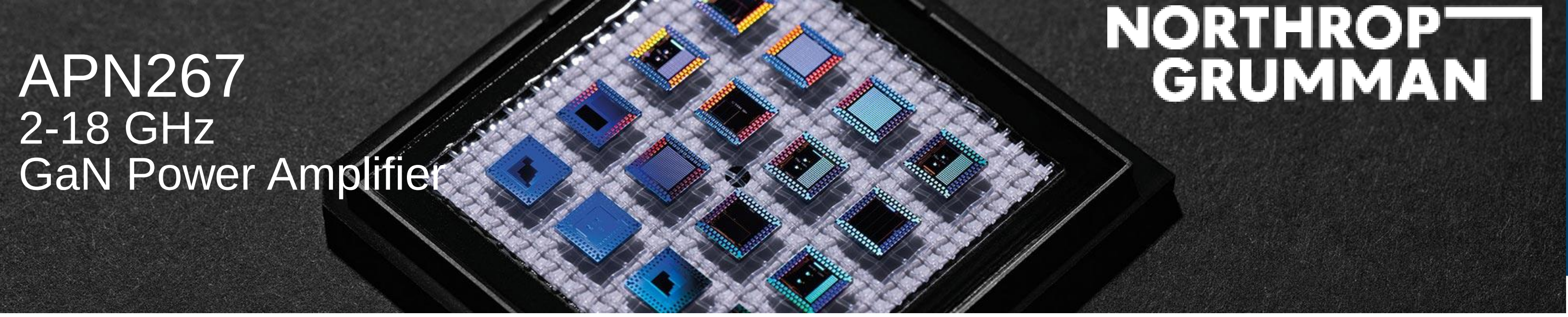
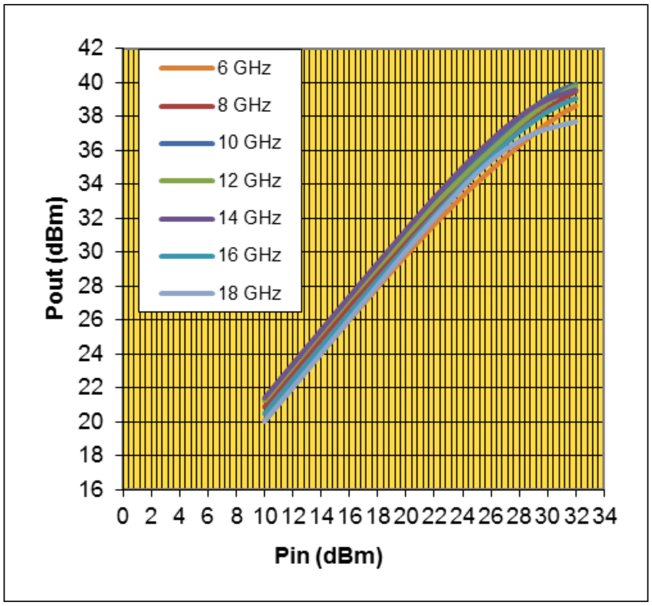


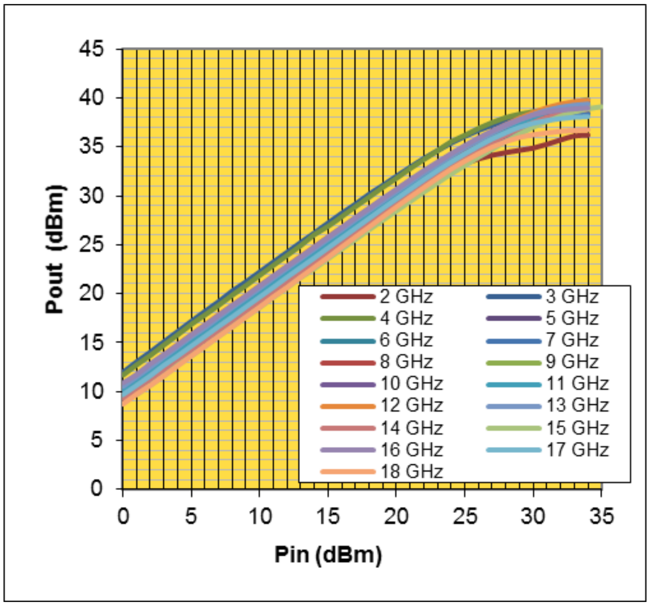
# APN267
## 2-18 GHz
## GaN Power Amplifier

**On wafer measured Performance Characteristics (Typical Performance at 25°C)**
**Vd = 24.0 V, Id1 + Id1a = 480 mA.**

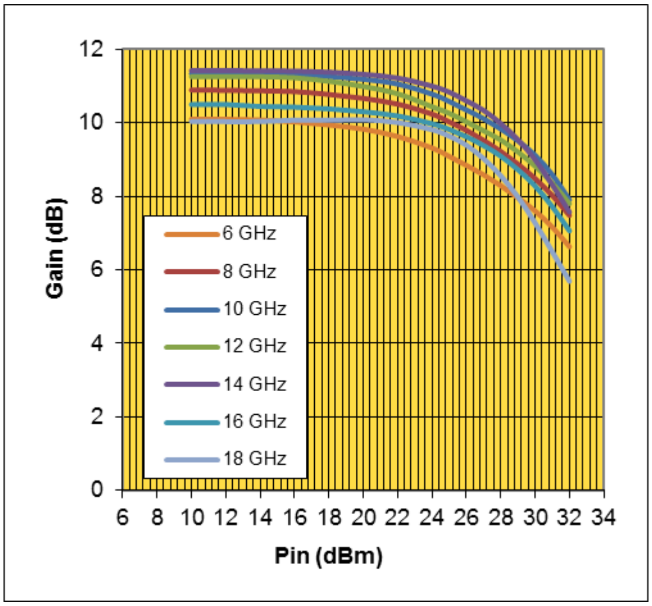
POUT vs. PIN*



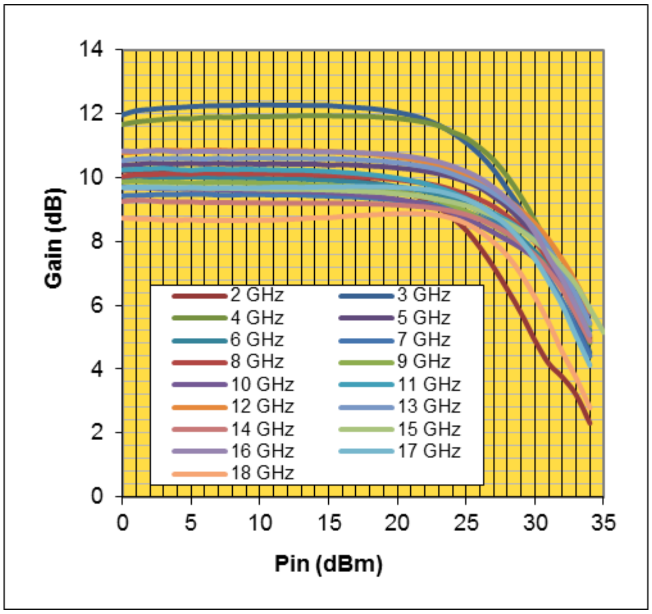

POUT vs. PIN **




GAIN vs PIN*




GAIN vs. PIN**




*Pulsed-power on-wafer

** CW fixtured





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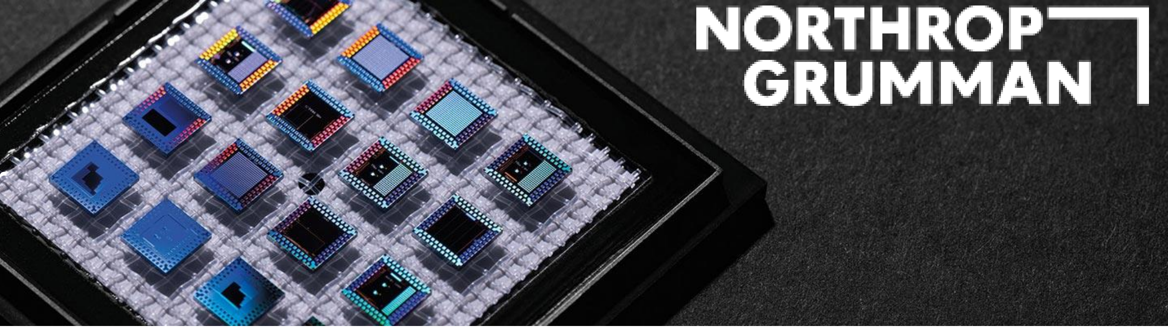
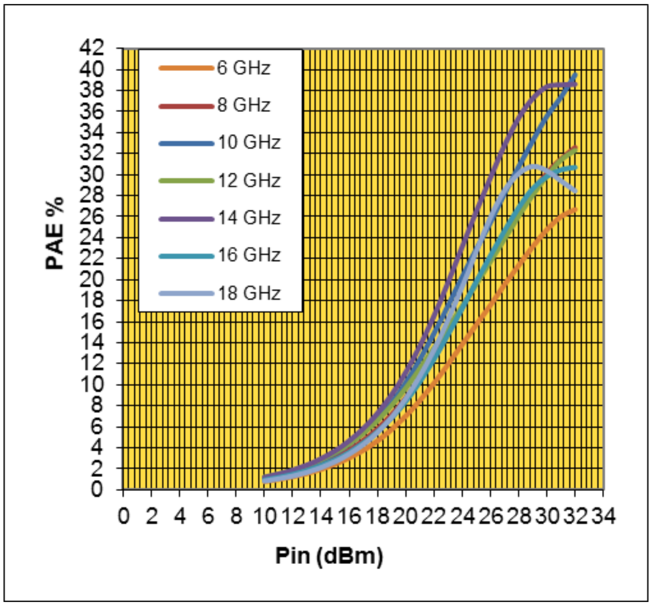
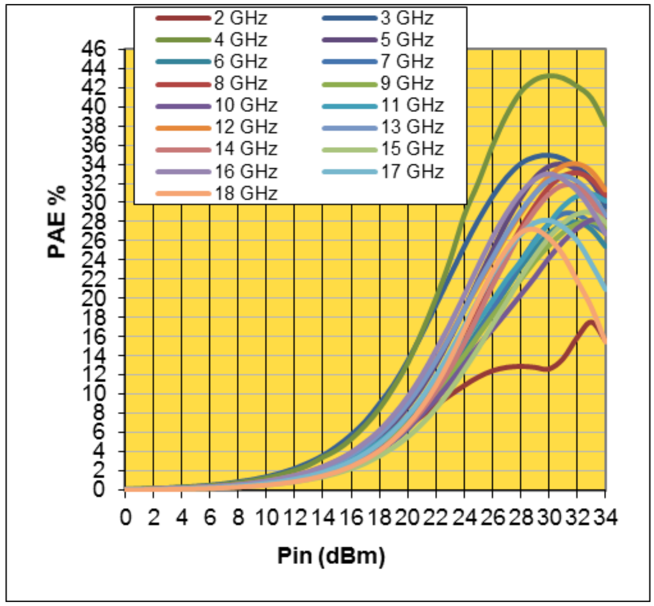


## On wafer measured Performance Characteristics (Typical Performance at 25°C)
## Vd = 24.0 V, Id1 + Id1a = 480 mA.

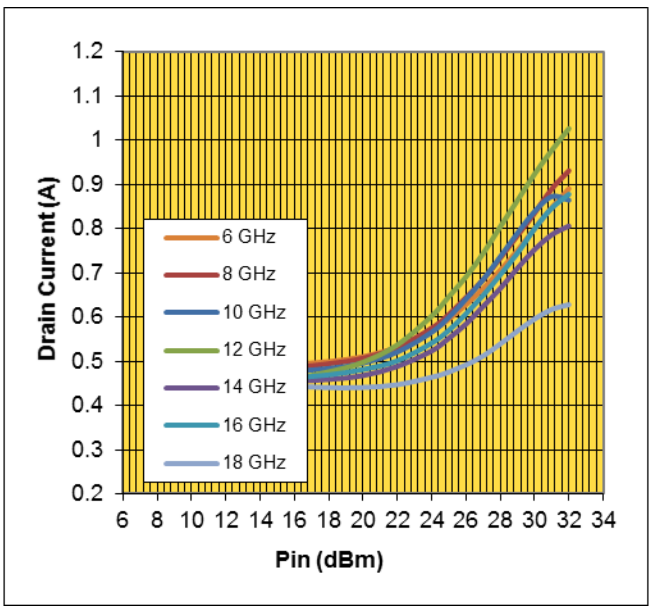
PAE vs. PIN*



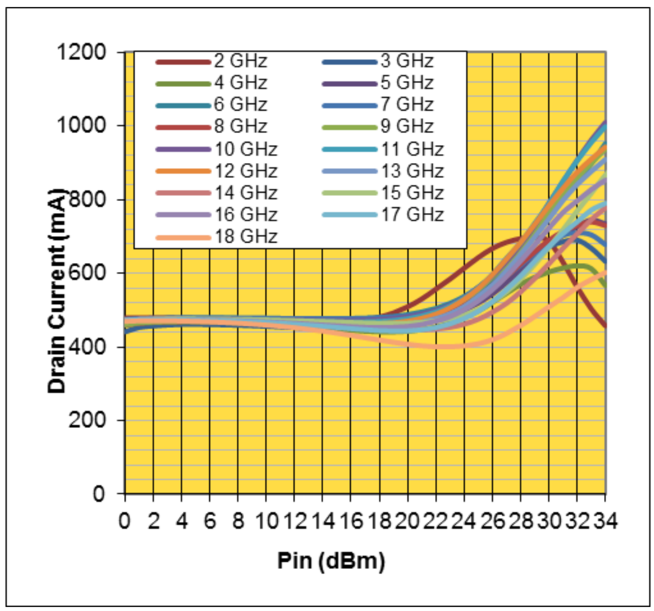

PAE vs. PIN **




Drain Current vs PIN*




Drain Current vs. PIN**




*Pulsed-power on-wafer

** CW fixtured



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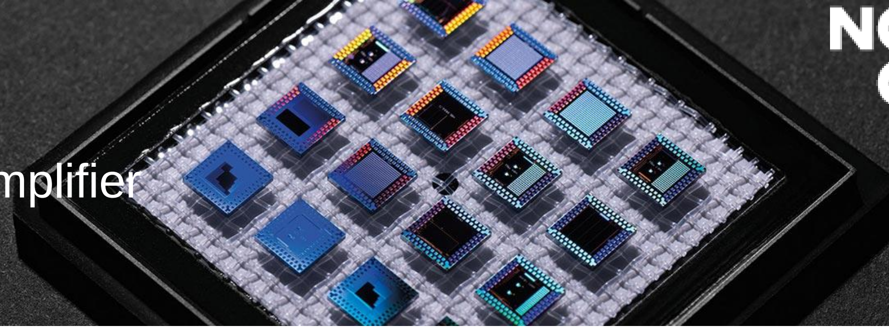

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## On wafer measured Performance Characteristics (Typical Performance at 25°C)
## Vd = 24.0 V, Id1 + Id1a = 480 mA.

| Freq GHz | S11 Mag | S11 Ang | S21 Mag | S21 Ang | S12 Mag | S12 Ang | S22 Mag | S22 Ang |
|---|---|---|---|---|---|---|---|---|
| 2.0 | 0.900 | -101.444 | 3.419 | -73.394 | 0.012 | -157.701 | 0.482 | 8.126 |
| 2.5 | 0.888 | -119.353 | 4.224 | -155.073 | 0.018 | 118.357 | 0.300 | -170.826 |
| 3.0 | 0.910 | -134.828 | 4.130 | 155.733 | 0.022 | 71.098 | 0.286 | 136.547 |
| 3.5 | 0.912 | -149.993 | 4.083 | 116.126 | 0.025 | 32.204 | 0.141 | 121.495 |
| 4.0 | 0.891 | -162.703 | 3.929 | 81.397 | 0.027 | -1.300 | 0.111 | -165.600 |
| 4.5 | 0.868 | -173.839 | 3.712 | 50.706 | 0.029 | -31.428 | 0.234 | -167.036 |
| 5.0 | 0.853 | 173.901 | 3.479 | 23.546 | 0.030 | -57.950 | 0.326 | 159.964 |
| 5.5 | 0.845 | 166.212 | 3.309 | -1.169 | 0.031 | -81.476 | 0.378 | 161.077 |
| 6.0 | 0.842 | 155.735 | 3.231 | -24.235 | 0.033 | -103.420 | 0.393 | 143.221 |
| 6.5 | 0.837 | 144.692 | 3.216 | -46.459 | 0.035 | -124.794 | 0.385 | 124.592 |
| 7.0 | 0.826 | 132.627 | 3.265 | -68.675 | 0.039 | -146.174 | 0.350 | 103.560 |
| 7.5 | 0.808 | 119.227 | 3.350 | -91.421 | 0.042 | -168.686 | 0.300 | 78.197 |
| 8.0 | 0.778 | 104.554 | 3.463 | -114.776 | 0.047 | 168.831 | 0.246 | 46.052 |
| 8.5 | 0.745 | 88.333 | 3.589 | -139.247 | 0.051 | 145.298 | 0.208 | 4.220 |
| 9.0 | 0.697 | 70.195 | 3.665 | -164.449 | 0.055 | 120.931 | 0.210 | -41.813 |
| 9.5 | 0.649 | 50.319 | 3.703 | 170.095 | 0.059 | 96.287 | 0.243 | -80.868 |
| 10.0 | 0.608 | 28.781 | 3.714 | 144.329 | 0.062 | 71.961 | 0.277 | -113.150 |
| 10.5 | 0.578 | 5.295 | 3.718 | 118.666 | 0.064 | 47.123 | 0.300 | -137.922 |
| 11.0 | 0.570 | -19.471 | 3.680 | 93.209 | 0.067 | 22.511 | 0.295 | -161.220 |
| 11.5 | 0.579 | -44.762 | 3.648 | 67.190 | 0.069 | -2.551 | 0.267 | 124.150 |
| 12.0 | 0.603 | -69.521 | 3.605 | 40.957 | 0.071 | -27.685 | 0.211 | 154.647 |
| 12.5 | 0.631 | -93.350 | 3.552 | 14.550 | 0.072 | -53.295 | 0.141 | 128.738 |
| 13.0 | 0.647 | -116.091 | 3.486 | -12.468 | 0.074 | -79.318 | 0.072 | 79.233 |
| 13.5 | 0.654 | -137.861 | 3.419 | -39.595 | 0.076 | -106.205 | 0.073 | -18.338 |
| 14.0 | 0.644 | -158.478 | 3.340 | -67.386 | 0.076 | -132.689 | 0.146 | -61.695 |
| 14.5 | 0.618 | -67.999 | 3.259 | -95.452 | 0.077 | -159.987 | 0.214 | -87.308 |
| 15.0 | 0.578 | 161.991 | 3.203 | -123.836 | 0.078 | 170.168 | 0.266 | -107.669 |
| 15.5 | 0.537 | 141.631 | 3.208 | -153.496 | 0.080 | 144.035 | 0.286 | -127.939 |
| 16.0 | 0.502 | 118.152 | 3.237 | 168.363 | 0.084 | 113.547 | 0.264 | -149.355 |
| 16.5 | 0.461 | 89.089 | 3.286 | 140.726 | 0.088 | 80.431 | 0.184 | -163.319 |
| 17.0 | 0.406 | 51.169 | 3.324 | 102.632 | 0.091 | 43.639 | 0.047 | 126.189 |
| 17.5 | 0.336 | 0.463 | 3.222 | 59.656 | 0.090 | 2.487 | 0.177 | -27.855 |
| 18.0 | 0.250 | -70.712 | 2.897 | 12.462 | 0.083 | -42.649 | 0.405 | -61.638 |



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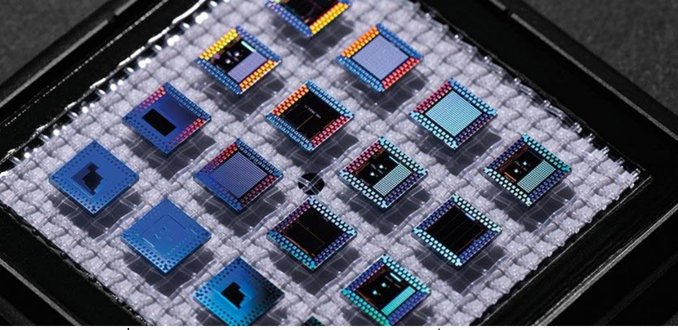

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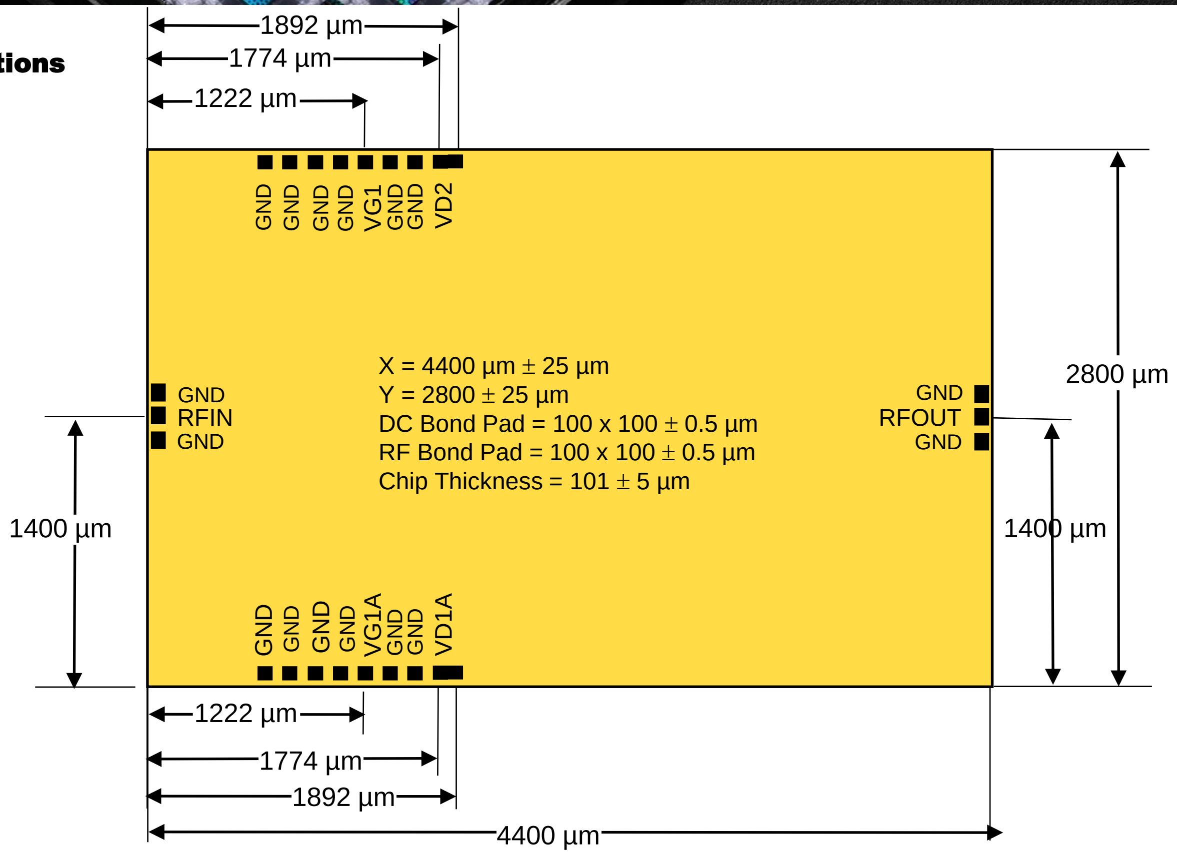
**Die Size and Bond Pad Locations**
**(Not to Scale)**




**Biasing/De-Biasing Details:**
Bias for 1st must be from both sides.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-5 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
    i. Gradually decrease drain bias to 0 V.
    ii. Gradually decrease gate bias to 0 V.
    iii. Turn off supply voltages





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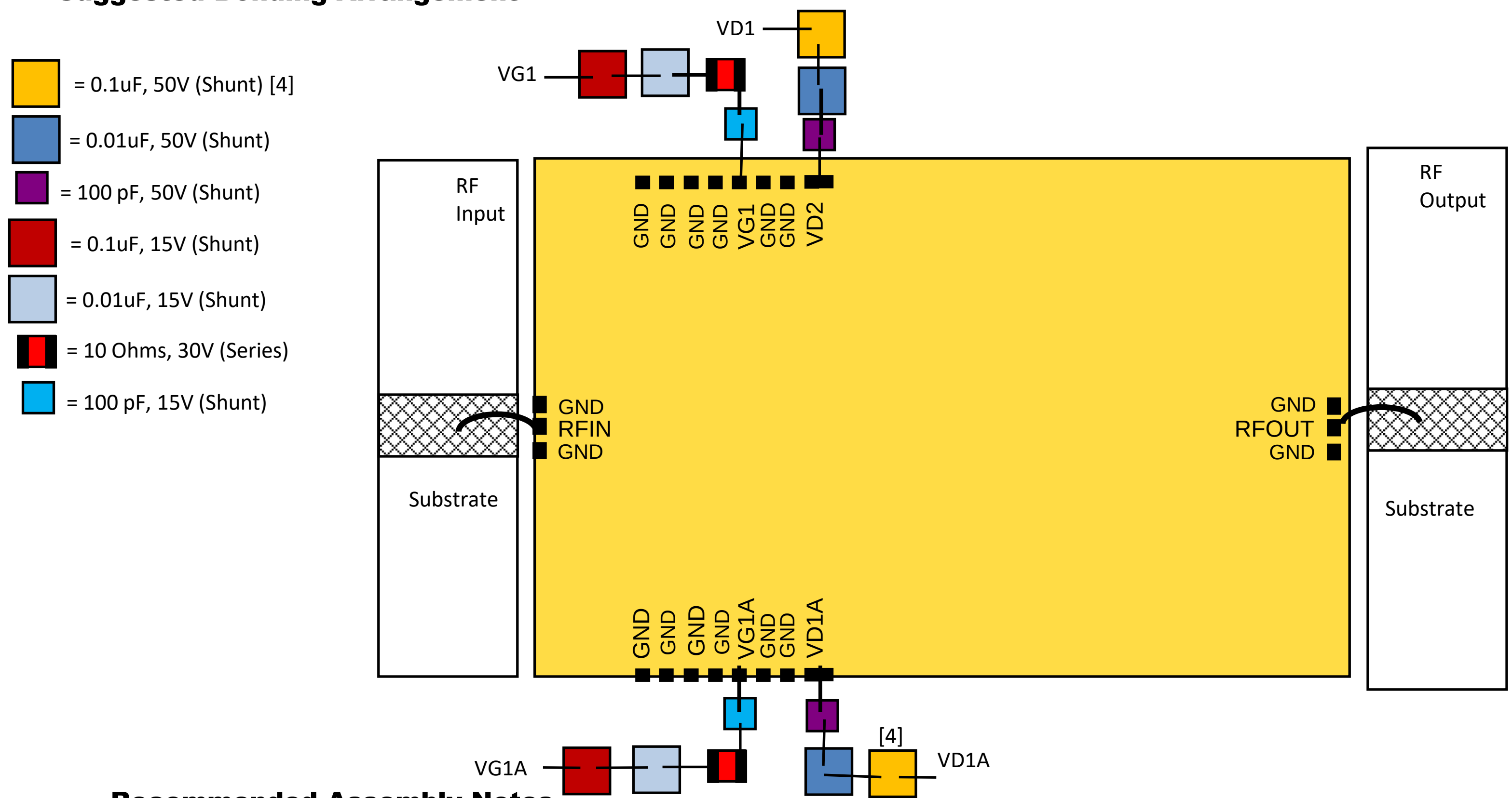
## Suggested Bonding Arrangement




## Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

## Mounting Processes

Most NGAS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320°C for 30 seconds.

**Note**: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

**CAUTION**: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

**PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!**